

Compal Confidential

DH5AV_JV_0V Schematics Document

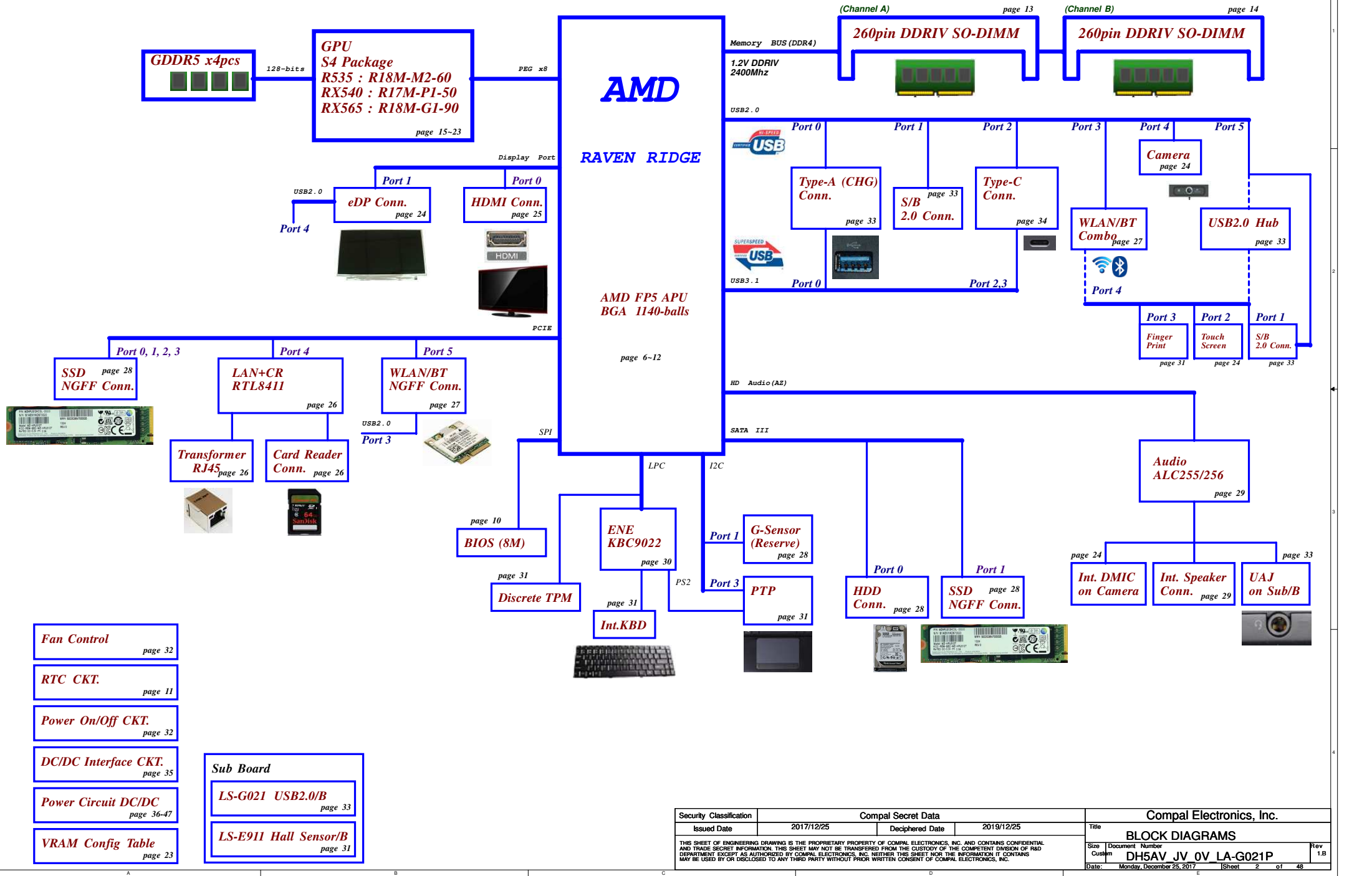
AMD Raven Ridge Platform

AMD R17M-P1-50/R18M-M1-60/R18M-G1-90

LA-G021P REV:1.8

2017-12-25

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				COVER PAGE	
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				Custom	DH5AV_JV_0V_LA-G021P
				Date:	Thursday, January 11, 2018
				Sheet	1 of 48
				Rev	1.8



Voltage Rails

Power Plane	Description	S0	S3	S5
+19V_VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.8VALW	0.8V always on power rail	ON	ON	OFF
+0.8VS	0.8V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail for APU and DDR	ON	ON	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+0.6VS	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	AC:ON DC:OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3V_LAN	3.3V LAN IC power	ON	ON	OFF
+TP_VCC	3.3V Touch Pad power	ON	ON	OFF
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+0.8VSDGPU	VGA power	ON	OFF	OFF
+VDDCI	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF
+FP_VCC	3.3V Finger Print power	ON	ON	OFF

APU SMBus/I2C Address Table

Master	Device	Address[7:1]	Address [7:0]	
			Write	Read
I2C Port 0 (+1.8VS)				
I2C Port 1 (+1.8VS)	G-Sensor (Reserver)	0001 1000b 18h	0011 0000b 30h	0011 0001b 31h
I2C Port 2 (+3VS)				
SBMbus Port 0 (+3VS)	JDIMM1	0101 0000b 50h	1010 0000b A0h	1010 0001b A1h
	JDIMM2	0101 0001b 51h	1010 0010b A2h	1010 0011b A3h
I2C Port 3 (+3VALW)	PTP (Synaptics)	0010 1100b 2Ch	0101 1000b 58h	0101 1001b 59h
	PTP (ELAN)	0001 1111b 15h	0011 1110b 3Eh	0011 1111b 3Fh
SMBus Port 1 (+3VALW)				

EC SMBus Address Table

SMBus Port 1 (+3VALW)	Smart Battery	0000 1011b 0Bh	0001 0110b 16h	0001 0111b 17h
	Charger IC (BQ24735)	0000 1001b 09h	0001 0010b 12h	0001 0011b 13h
SMBus Port 2 (+3VS)	APU Temp. (TSI)	0100 1100b 4Ch	1001 1000b 98h	1001 1001b 99h
	GPU Temp.	0100 0001b 41h	1000 0010b 82h	1000 0011b 83h
	CC-Logic	1100 0000b C0h	1000 0000b 80h	1000 0001b 81h

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	DH5JV
2	DH5AV
3	DH50V

ZZZ @
DA8001E9010
PCB 28Z LA-G021P REV1 MB 2
ZZZ PCB@
DAZ28200100
PCB DH5JV LA-G021P LS-G021P/E911P
ZZZ PCB1@
DAZ28200101
PCB DH5JV LA-G021P LS-G021P/E911P 1A
ZZZ PCB1@
DAZ28200102
PCB DH5JV LA-G021P LS-G021P/E911P 1B

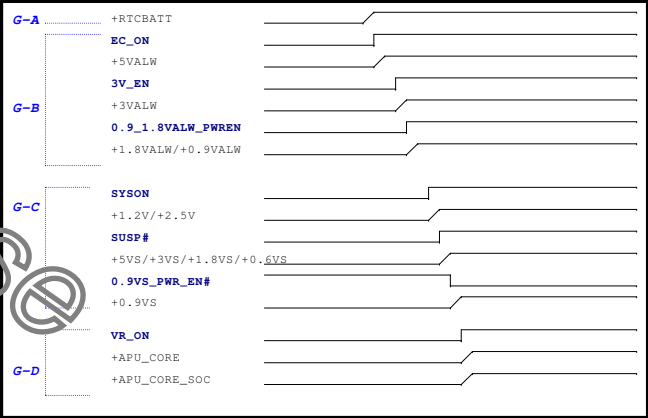
BOM Structure Table

BOM Structure	BTO Item
@	Unpop
EMC@/EMC@	EMI/ESD Pop/Unpop
4F@	HDMI Royalty
CONN@	Mechanical Connector
JP@	Jump
RS@	R-Short
TP@	Test Point
TPM@	TPM Circuits
PCIE@/T1PCIE@	PCIE 8000/1 APU PCIE SSD
SATA@	SATA SSD
GS@	G-Sensor Circuits
LDO@/SWR@	RTL8411 LED Mode/Switching Mode
PAR@/TI@	SATA Redrive PARADE/Tristation
CHG@/NCHG@	USB Charger/Non-Charger
255@	Audio Codec AL255 Design
256@/256EMC@	Audio Codec AL256 Design
UMA@	UMA Config
R3/R5/R7APU@	APU PN Refer p.6
15W@/25W@/35W@	APU Watt Config
T1@/T2@	APU Type Config
EJ@/EA@/VX@	EJ/EA/VX Project Config
DIS@/T1DIS@	VGA Circuits/Type1-APU VGA Circuits
	GPU and VRAM Config Refer p.23
R535@	R18M-M2-60 GPU
RX540@	R17M-P1-50 GPU
RX565@	R18M-G1-90 GPU
LEXA@	LEXA Series VGA
VRAM7G@/VRAM6G@	VRAM7G and VRAM6G
HUB@/NHUB@	USB20 HUB/Non-HUB
FP@/FP@EMC@	Finger Print
DMIC2@/DMIC4@	2 or 4 DMIC Design
HDT@	HDT Circuits
TYPEC@	TYPEC Circuits
TYPECEMC@	TYPEC EMC Circuits
NTYPEC@	No TYPEC Circuits

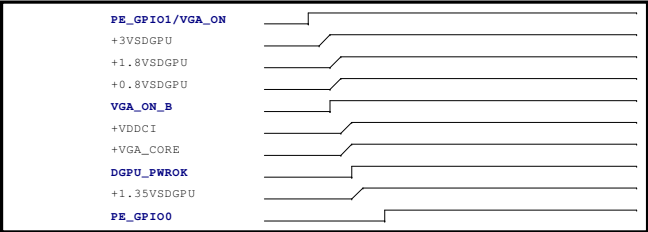
Board ID / SKU ID Table for AD channel

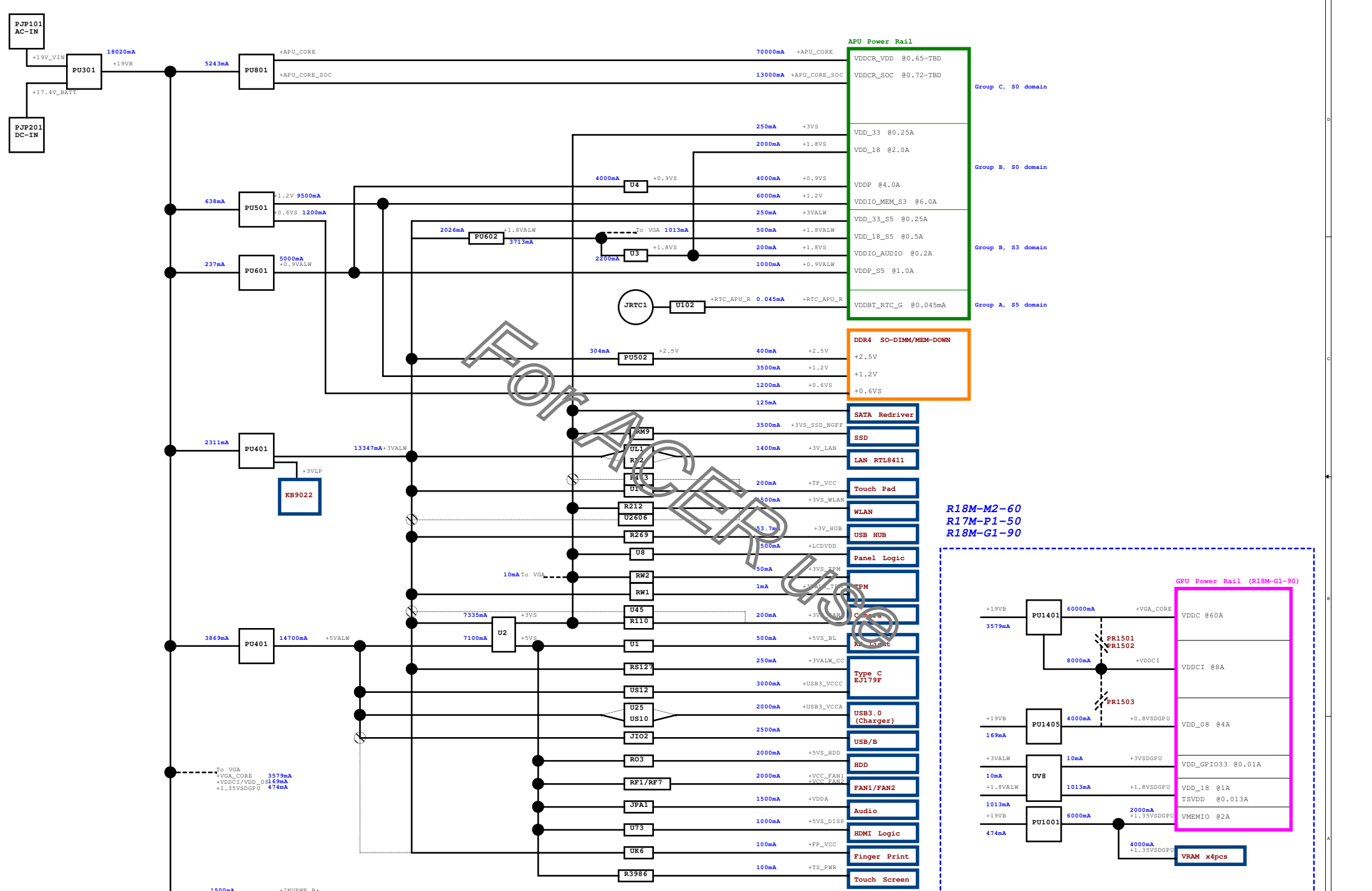
Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

POWER SEQUENCE



VGA POWER SEQUENCE



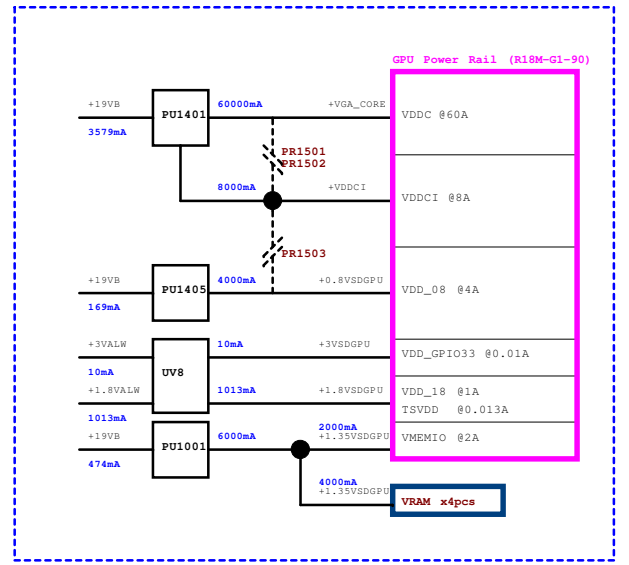


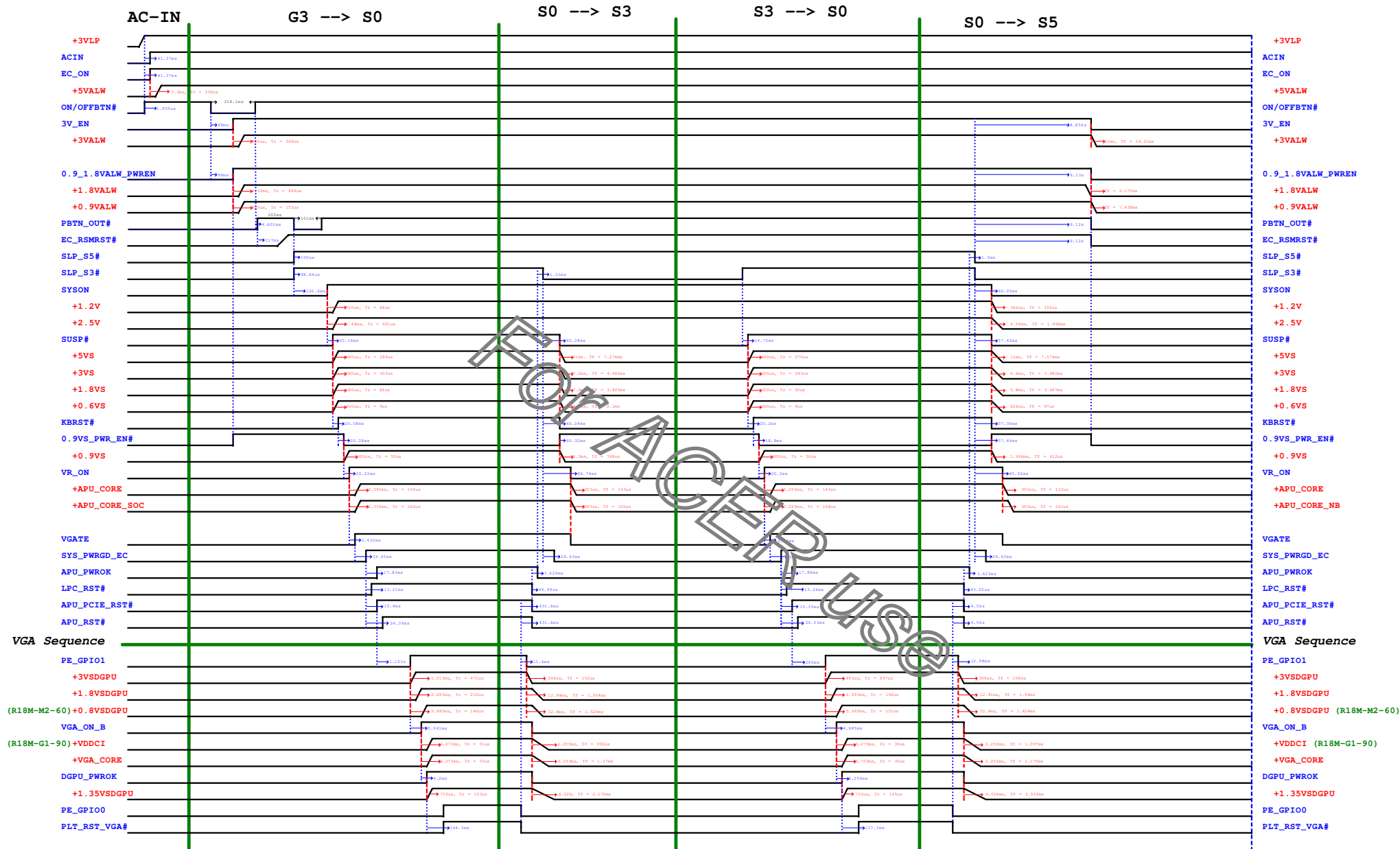
APU Power Rail	
VDDCR_VDD @0.65-TBD	
VDDCR_SOC @0.72-TBD	
VDD_33 @0.25A	
VDD_18 @2.0A	
VDDP @4.0A	
VDDIO_MEM_S3 @6.0A	
VDD_33_S5 @0.25A	
VDD_18_S5 @0.5A	
VDDIO_AUDIO @0.2A	
VDDP_S5 @1.0A	
VDDBT_RTC_G @0.045mA	

DDR4 SO-DIMM/MEM-DOWN	
+2.5V	
+1.2V	
+0.6VS	

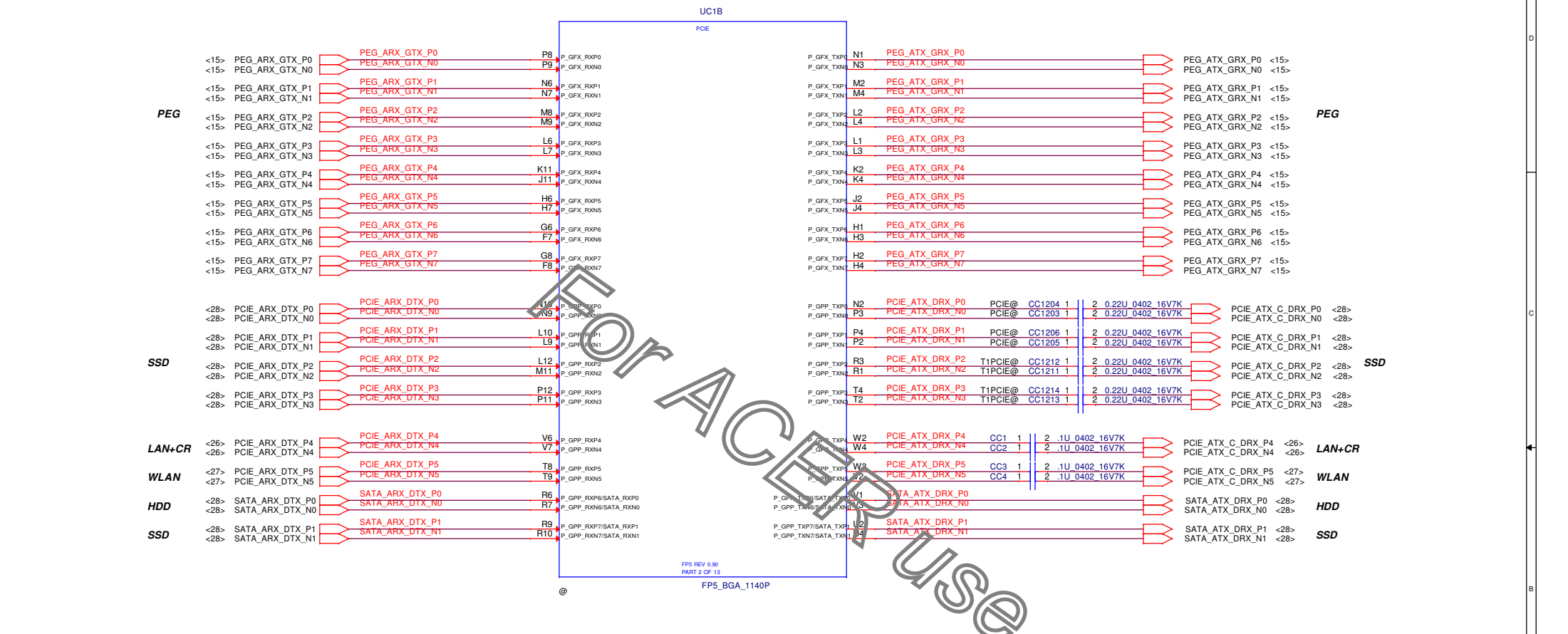
- SATA Redriver
- SSD
- LAN RTL8411
- Touch Pad
- WLAN
- USB HUB
- Panel Logic
- TPM
- Camera
- Keypad
- Type C EU179F
- USB3_0 (Charger)
- USB/B
- HDD
- FAN1/FAN2
- Audio
- HDMI Logic
- Finger Print
- Touch Screen

R18M-M2-60
R17M-P1-50
R18M-G1-90









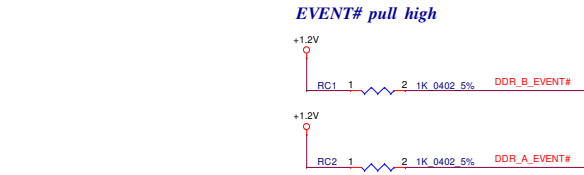
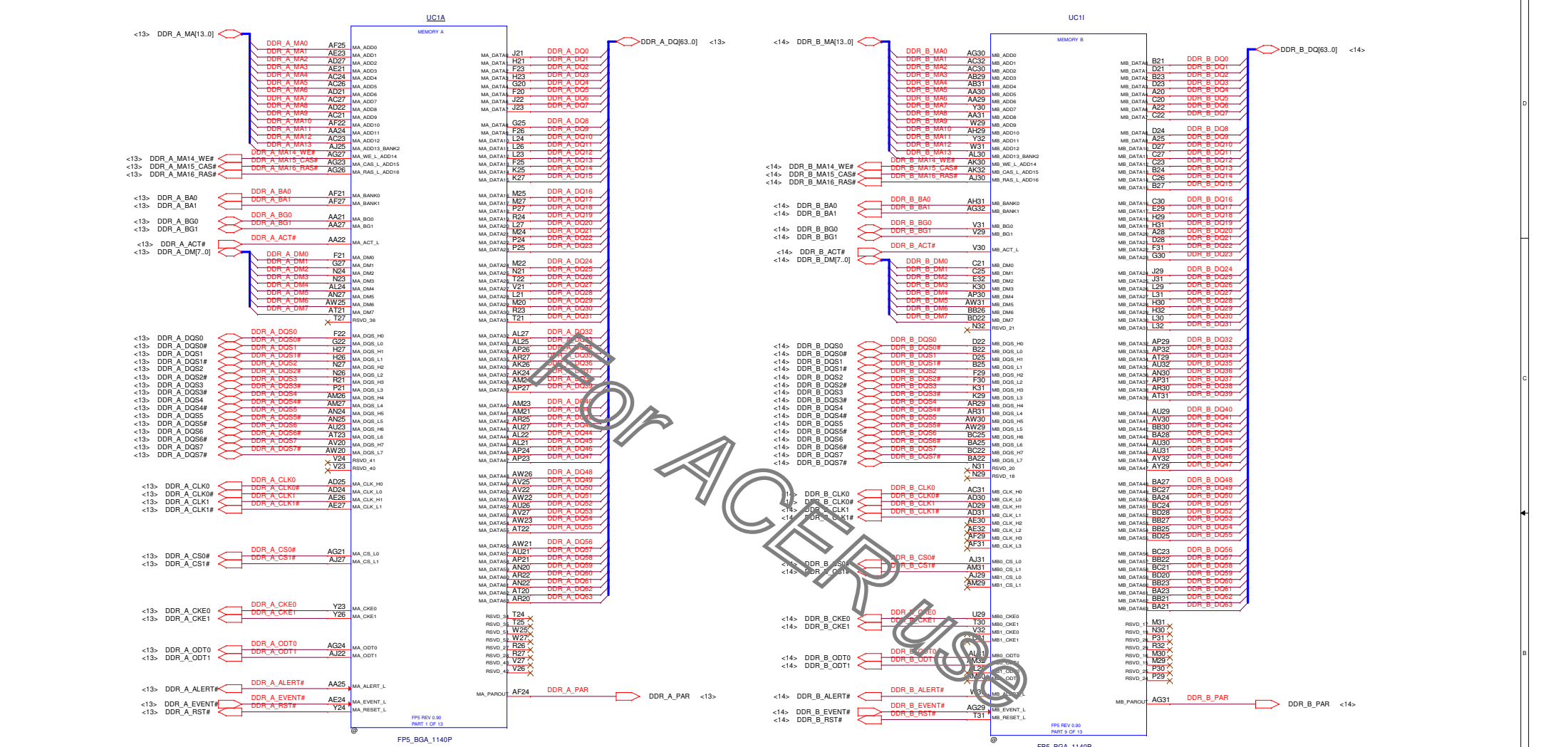
Main Func = CPU



APU PN Table

APU Platform	R3 PN	R3 PN	R3 PN	R3 PN
Raven	UC1 R3APUDC@	UC1 R3APUQC@	UC1 R5APU@	UC1 R7APU@
				
	S IC RAVEN3 YM2200C4T2OFB 2G BGA ABO!	S IC RAVEN3 YM2300C4T4MFB 2G BGA ABO!	S IC RAVEN5 YM2500C4T4MFB 2G BGA ABO!	S IC RAVEN7 YM2700C4T4MFB 2.2G BGA ABO!
	SA0000BBJ30	SA0000BIT20	SA0000A8R30	SA0000ASA20

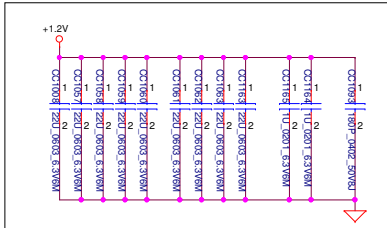
Main Func = CPU



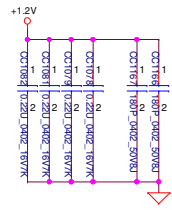
Main Func = CPU

```
+APU_CORE_SOC Cap  
place at Power Side
```

SCL/MBDG:
7*22uF (BU)
1*1uF (BU)
1*180pF (BU)

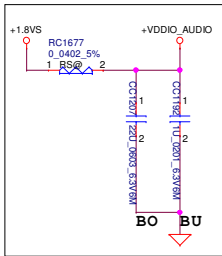


All BU(on bottom side under SOC)

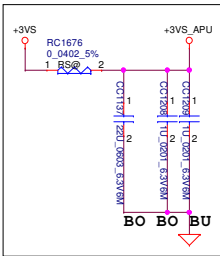


ACROSS VDDIO AND VSS SPLIT

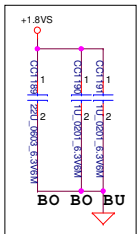
SCL/MBDG:
9*22uF (BU)
2*1uF (BU)
4*0.22uF
1*180pF (BU)
2*180pF



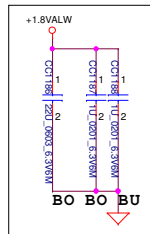
```
SCL/MBDG:
  1 *22uF (BO)
  1*1uF (BU)
```



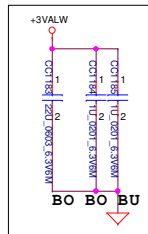
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



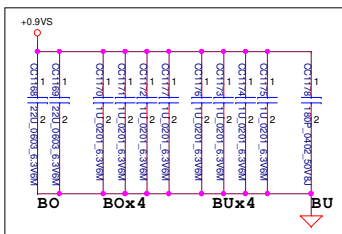
+1.8VALW



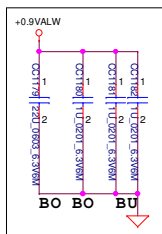
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



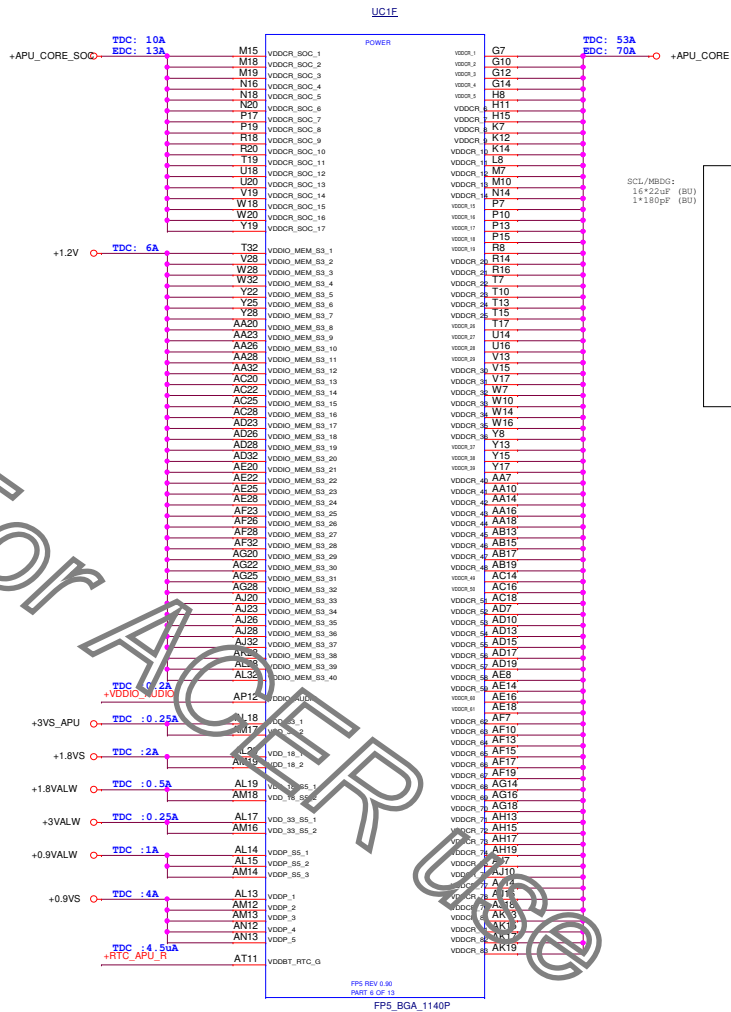
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



SCL/MBDG:
2 *22uF (BO)
8*1uF (BOx4+BUx4)
1*180pF (BU)

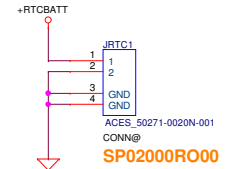


SCL/MBDG:
1 *22uF (BO)
3*1uF (BOx1+BUx2)

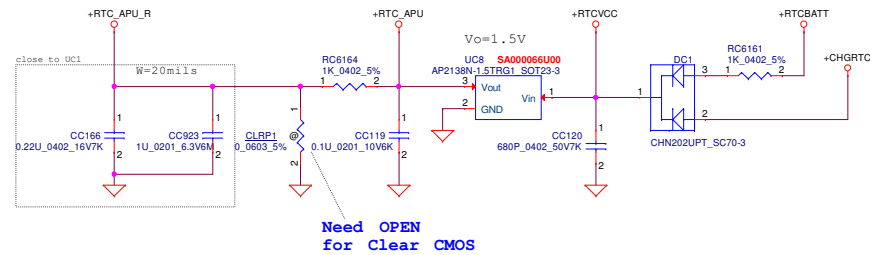


```
+APU_CORE Cap place at Power Side
```

SCL/MBDG:
16*22uF (BU)
1*180pF (BU)



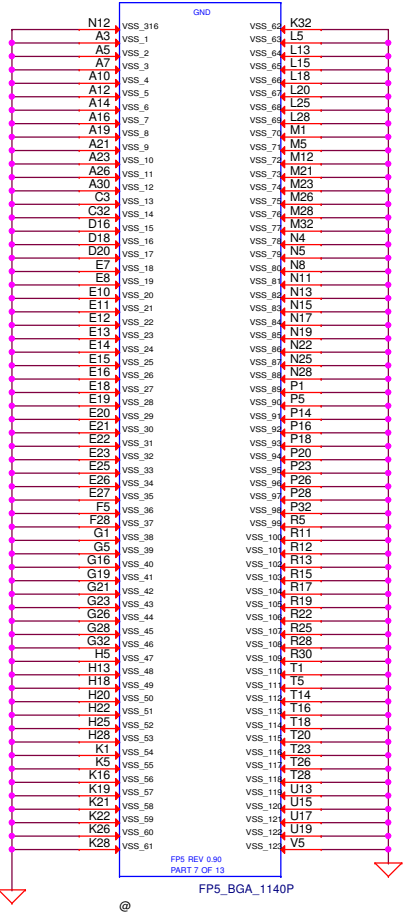
RTC OF APU



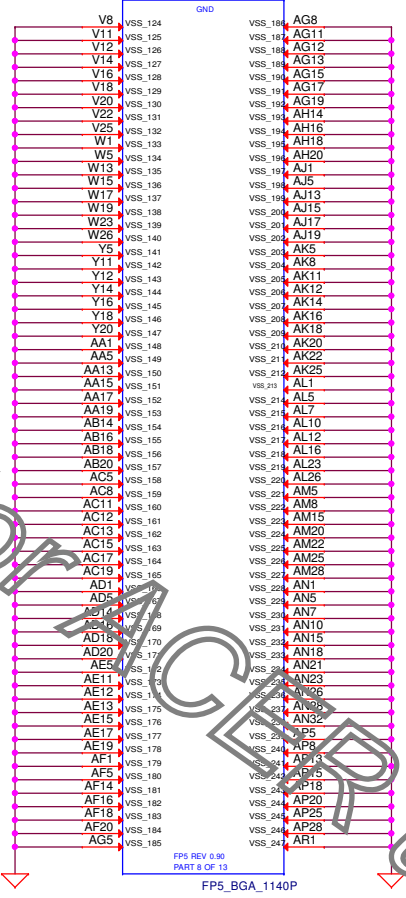
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Main Func = CPU

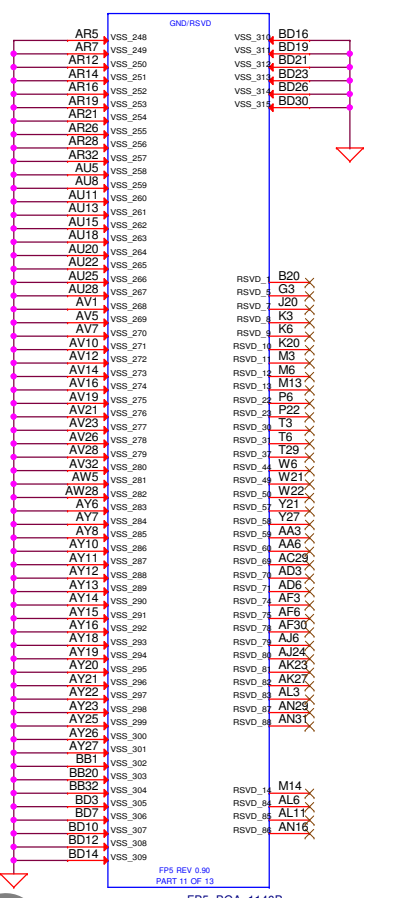
UC1G



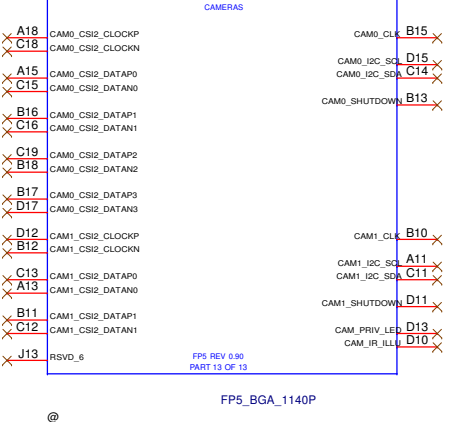
UC1H



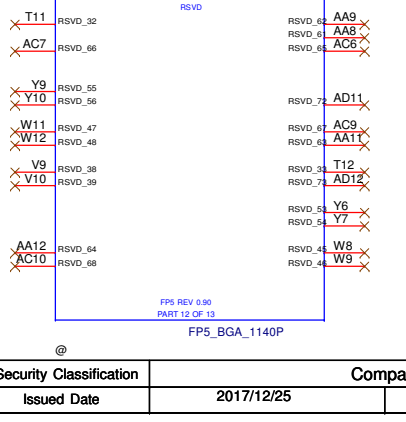
UC1K



UC1M



UC1L



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2-3A to 1 DIMMs/channel

The diagram shows three parallel power planes connected to a +3V3 supply at the top and ground at the bottom. Each plane contains three resistors (R7, R8, R9 in the top plane; R10, R11, R12 in the middle plane; R13, R14, R15 in the bottom plane) connected in parallel. The planes are connected to DDR_A_S#2, DDR_A_S#1, and DDR_A_S#0 respectively.

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

DDR4 support Even Parity check in DRAMs.

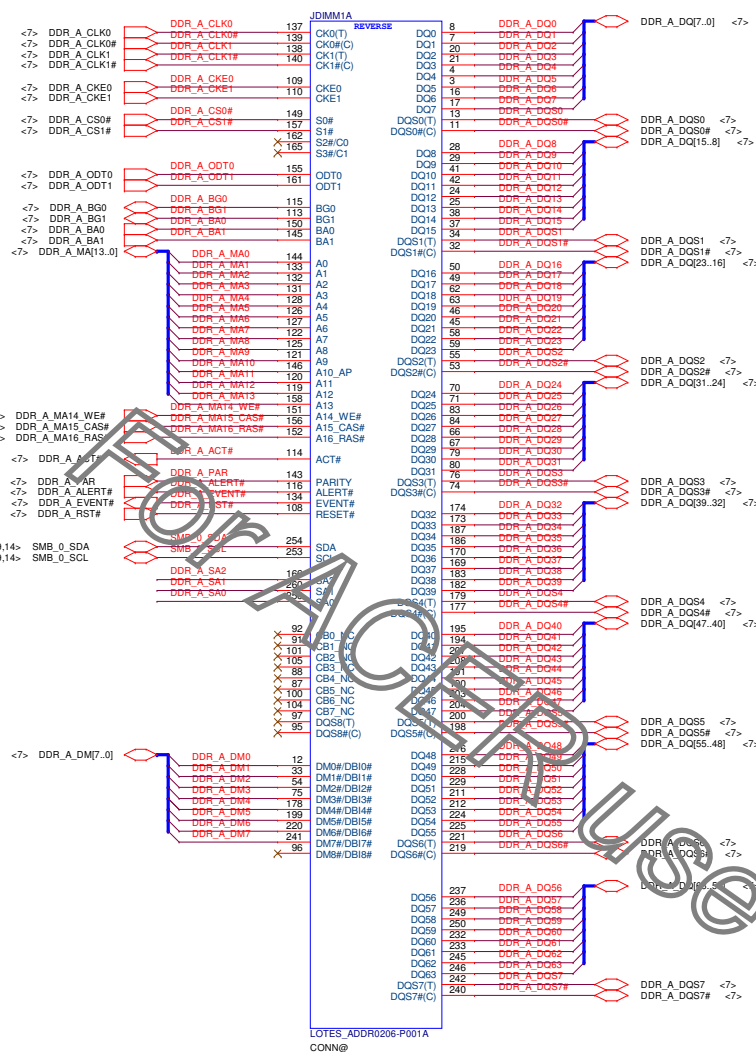
CRB use 0.1uF x12 (6 pop, 6 unpop), 180pF x1, 100uF x2

Follow MA51

1 @
+ CD18
330U_D2_2V_Y

2 SGA00009S00
330U 2V H1.9
9mohm POLY

A circuit diagram showing a 1uF capacitor connected to a +3VS source and ground. The capacitor is labeled '1u_0201_6.3V6M' and 'CD26'. The source is labeled '+3VS' and the ground is labeled 'GND'.

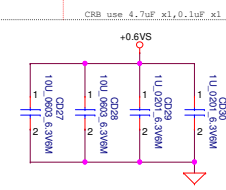


Follow CRB design

15mil

Place near to SO-DIMM connector.

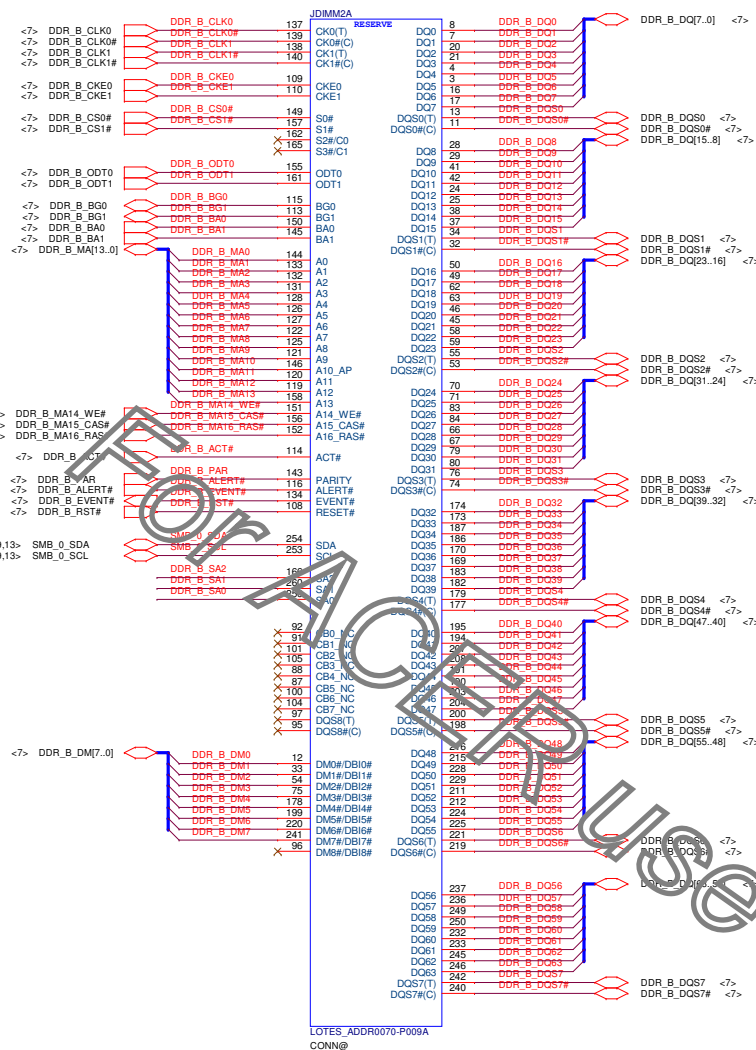
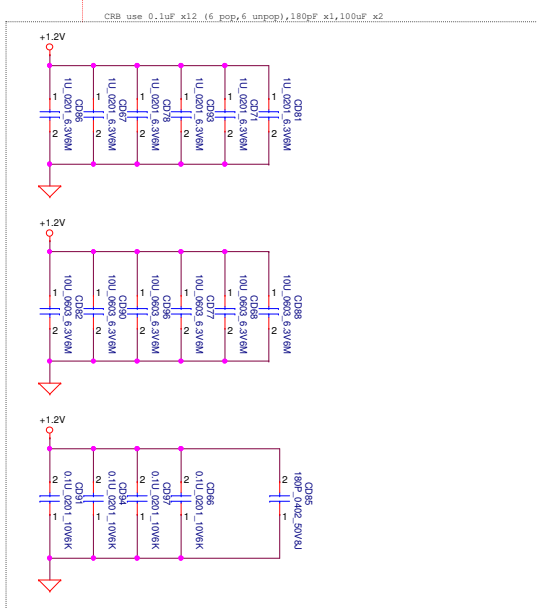
Layout Note:
Place near JDIMM1.258



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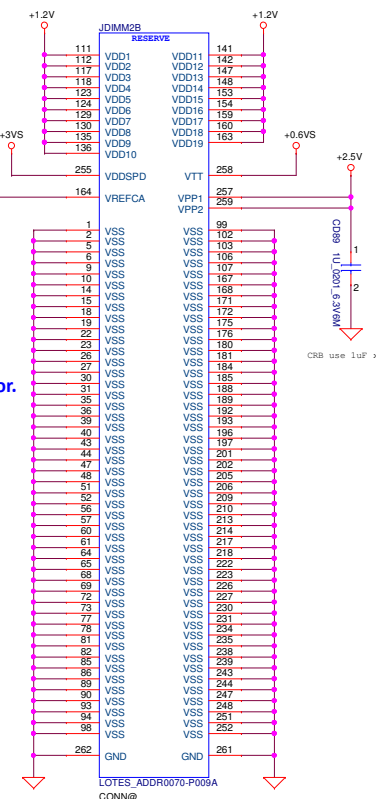
2-3A	to 1 DIMMs/channel
------	--------------------

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



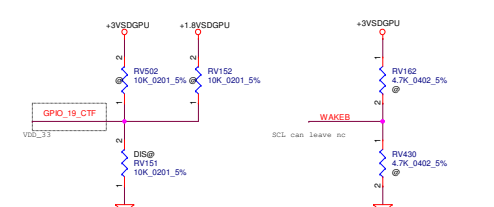
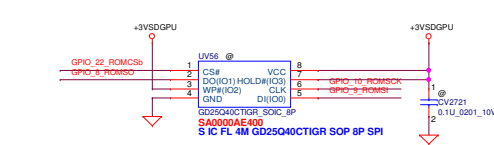
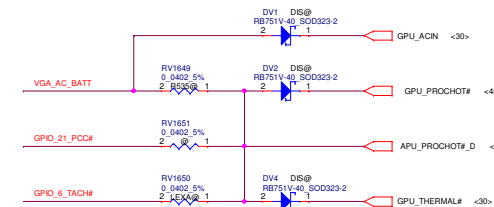
The schematic shows the connection for the +VREFB_CA pin. A 1.2V supply is connected through resistor RD243 (1K_0402_1%) to the top of capacitor CD76 (0.1μF, 0805-10V6K). The bottom of CD76 is connected to the +VREFB_CA pin. This node is also connected to the top of capacitor CD77 (1000pF, 0402-50V7K) and the top of capacitor CD80 (0.1μF, 0805-10V6K). The bottom of CD77 is connected to the top of capacitor CD81 (4.7μF, 0402-5.5V6K), which is then connected to ground. A 15mil dimension is indicated between the +VREFB_CA pin and the junction of CD77 and CD81.

Place near to SO-DIMM connector.

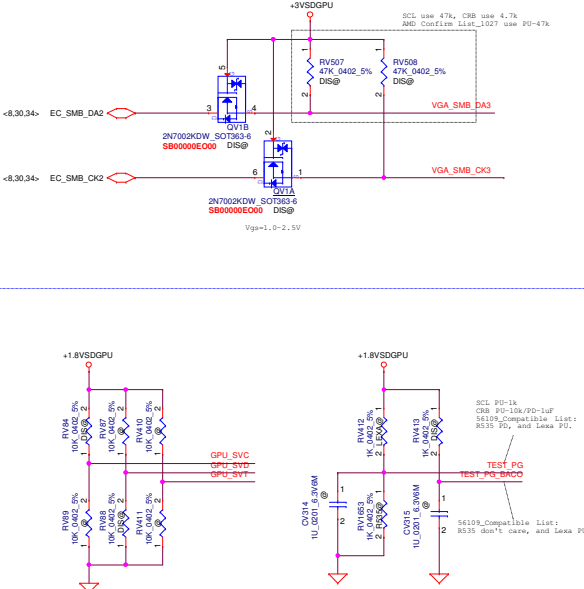


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Function Support	Pin	R18M-M2-60	R176-21-59/75 R176-21-59/75 R18M-G1-95
AC/DC Mode HAC LDC	GP105	Yes	Yes
Thermal_VR_HOT# (Fan tachometer)	GP106	No	Yes
Peak Current Control	GP1021	No	Yes



For ACER Use



Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

LEXA Strap

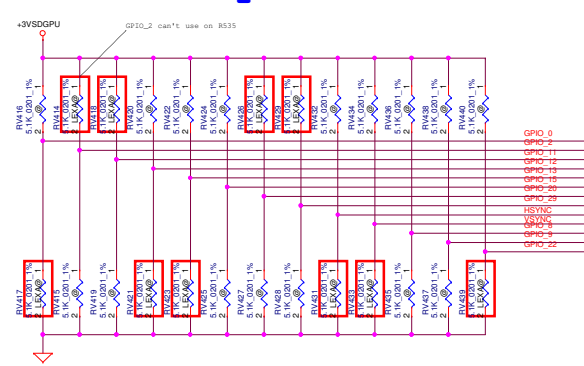


Table 3-27 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

3.2.2.2 ROM Configurations

- For designs that have a dedicated ROM device for the GPU video BIOS:
- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
 - Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).

R535 Strap

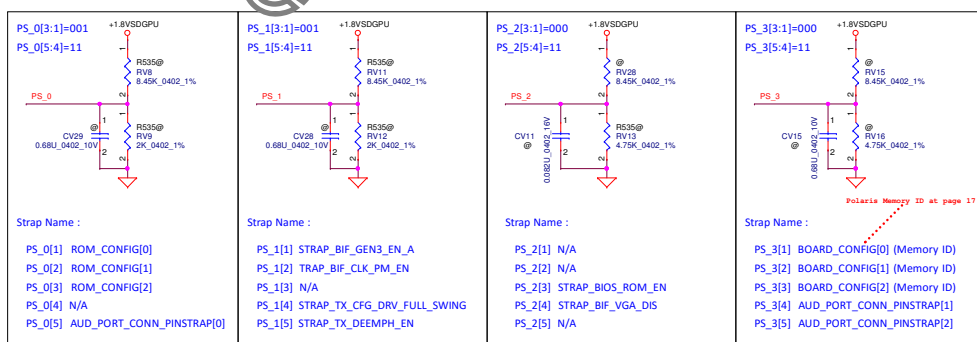
Resistor Divider Lookup Table

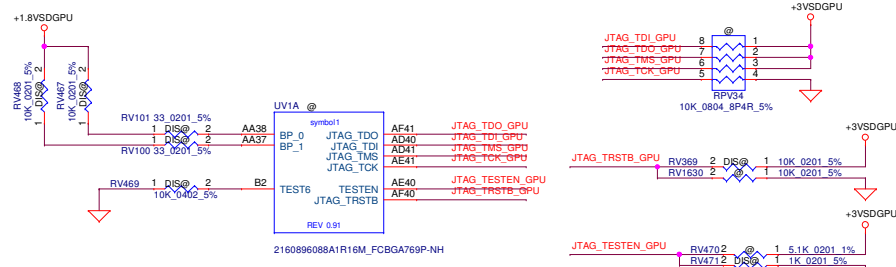
0402 1% resistors are required

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

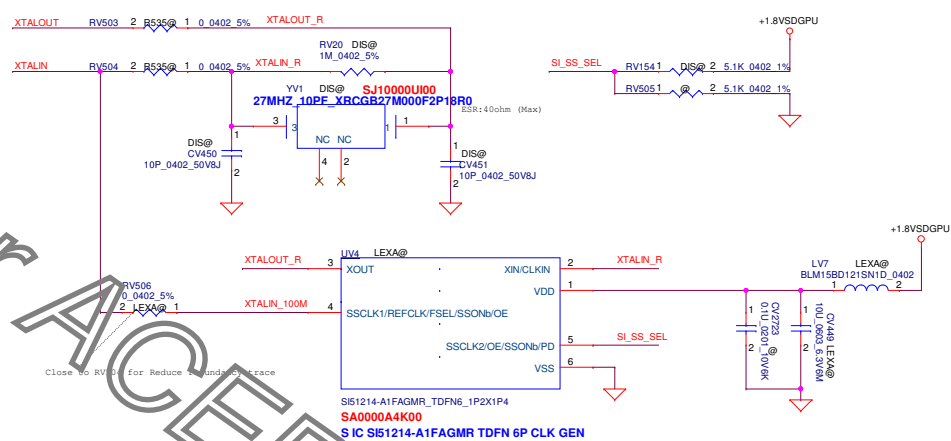
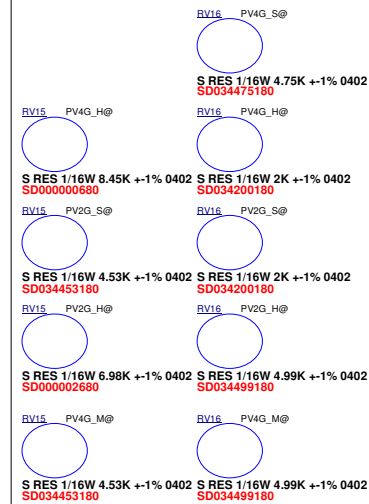
Capacitor Divider Lookup Table

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

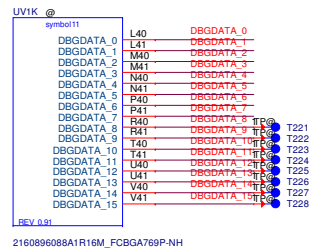




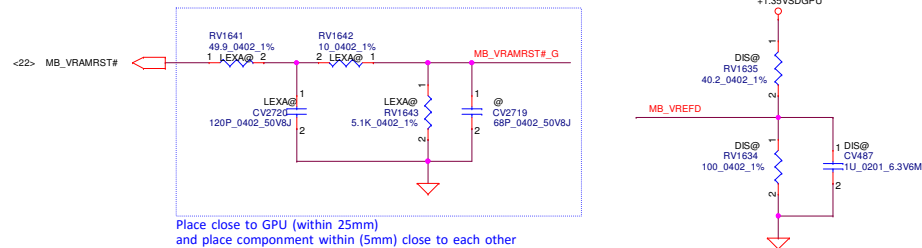
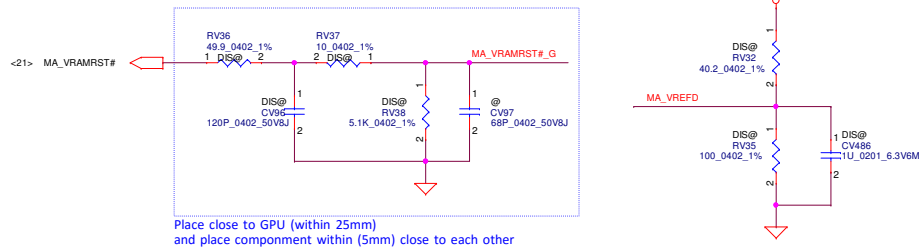
Polaris Memory ID



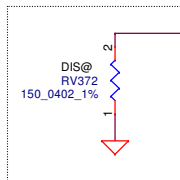
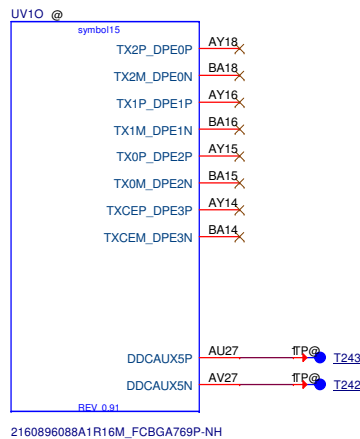
LEXA Memory ID



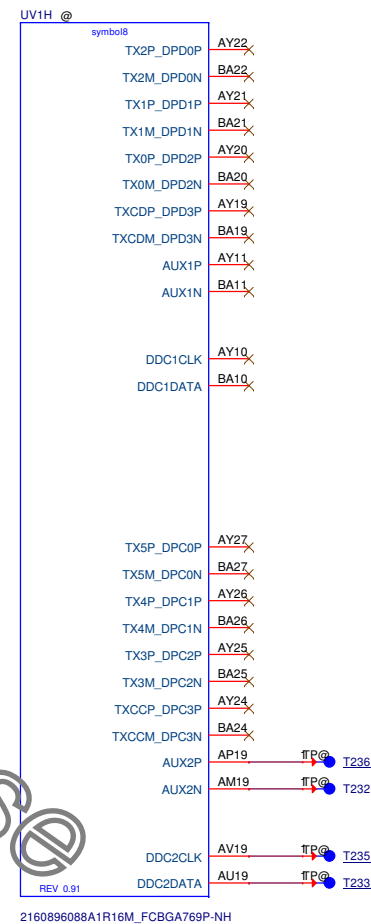
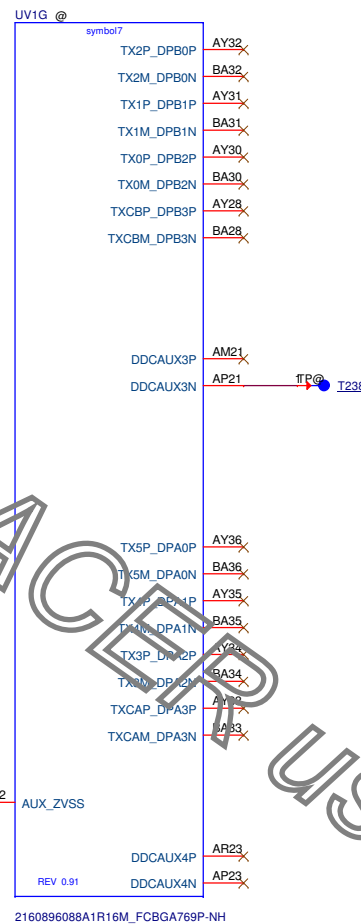
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Issued Date	2017/12/25	Deciphered Date	2019/12/25	Title	R18M-M260/G190 (3/9) MSIC-2
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				Custom	DH5AV JV 0V LA-G021P Date: Monday, December 25, 2017 Sheet 17 of 48



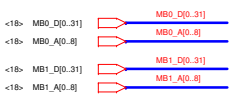
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Issued Date		2017/12/25		Deciphered Date		2019/12/25			
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				R18M-M260/G190 (4/9) MEM					
				Size		Document Number		Rev	
				Customer		DH5AV JV 0V LA-G021P		1.8	
				Date:		Monday, December 25, 2017		Sheet	



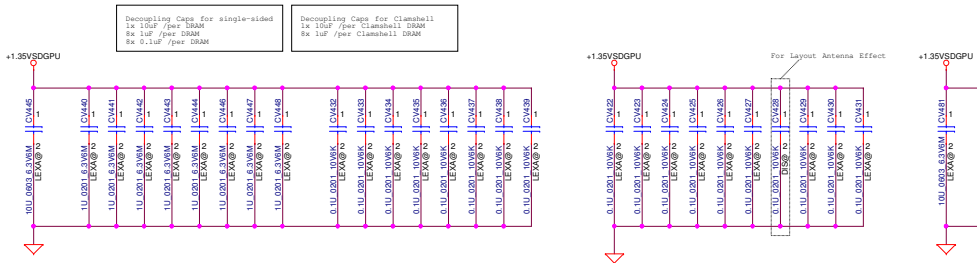
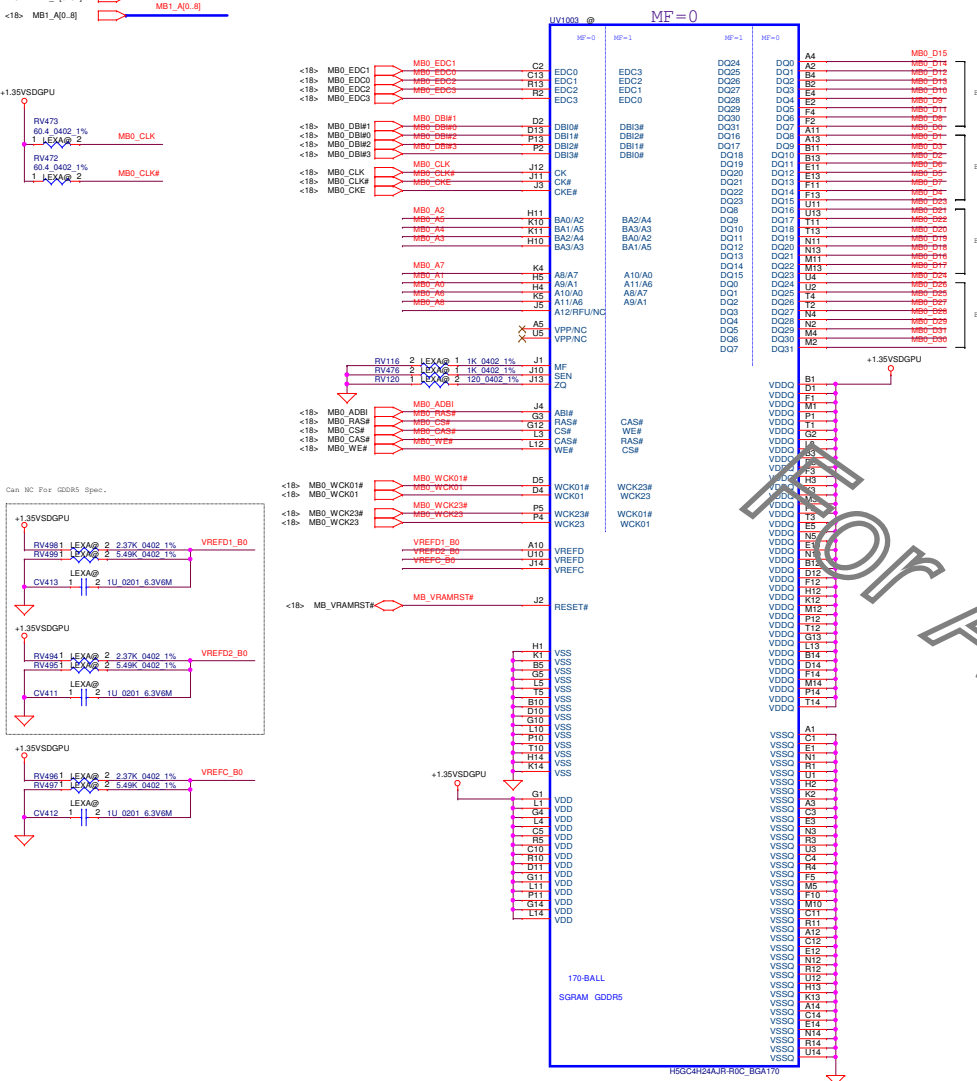
Data Book: need config even if not use display function



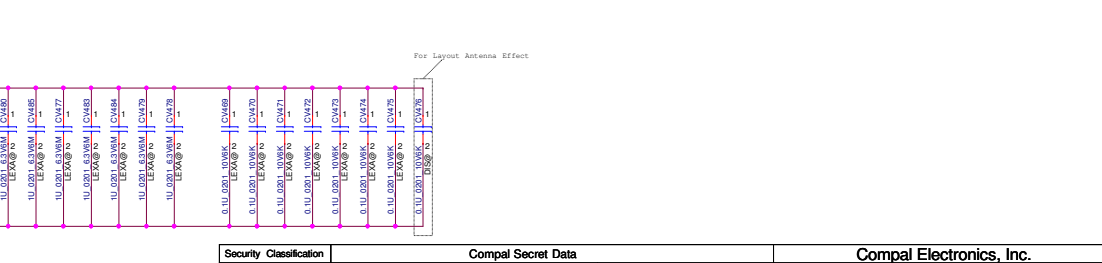
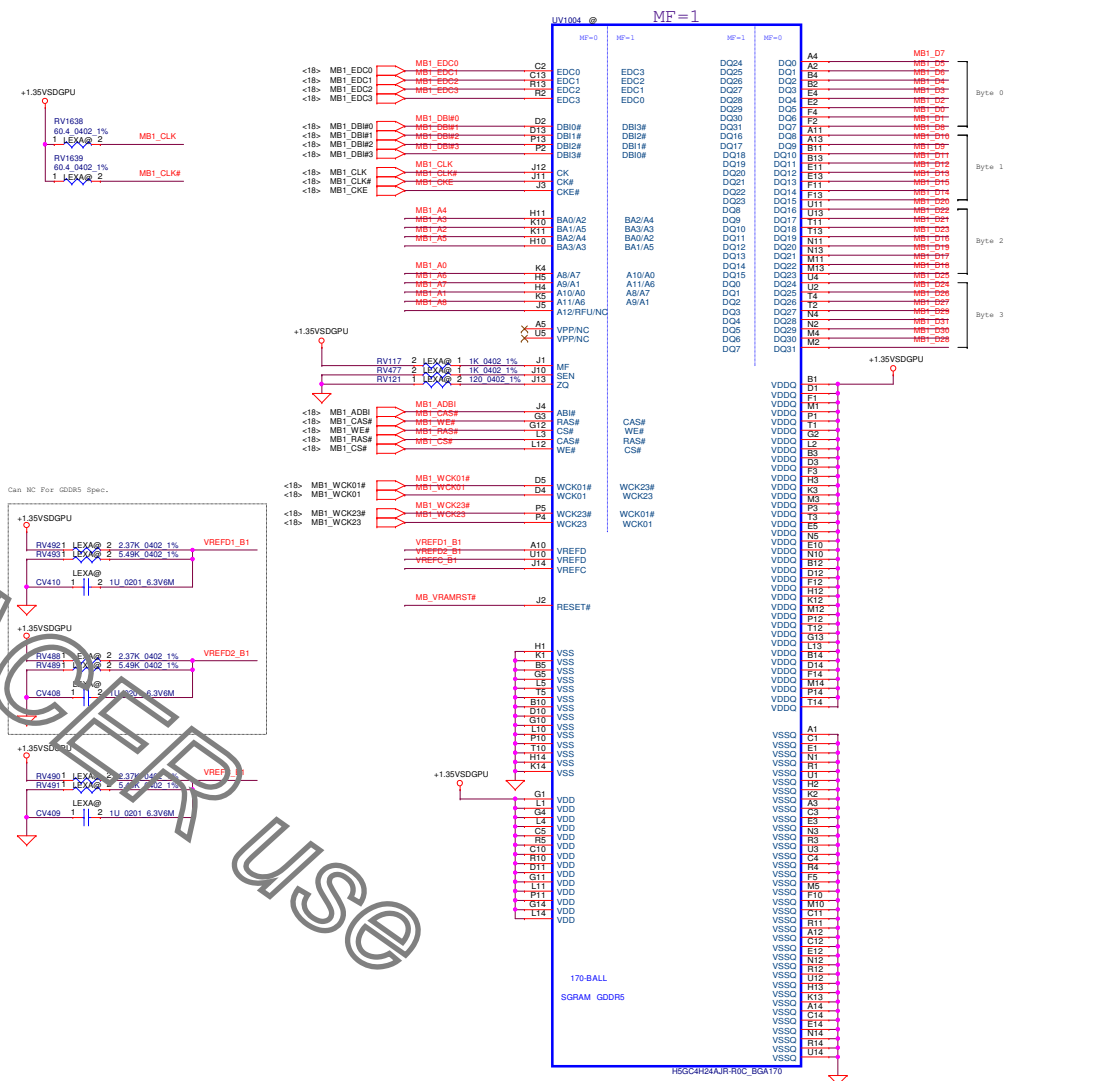
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Issued Date	2017/12/25	Deciphered Date	2019/12/25	Title	
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Size		Document Number		Rev	
Custom		DH5AV_JV_0V_LA-G021P		1.8	
Date:		Monday, December 25, 2017		Sheet 19 of 48	



B0 Channel



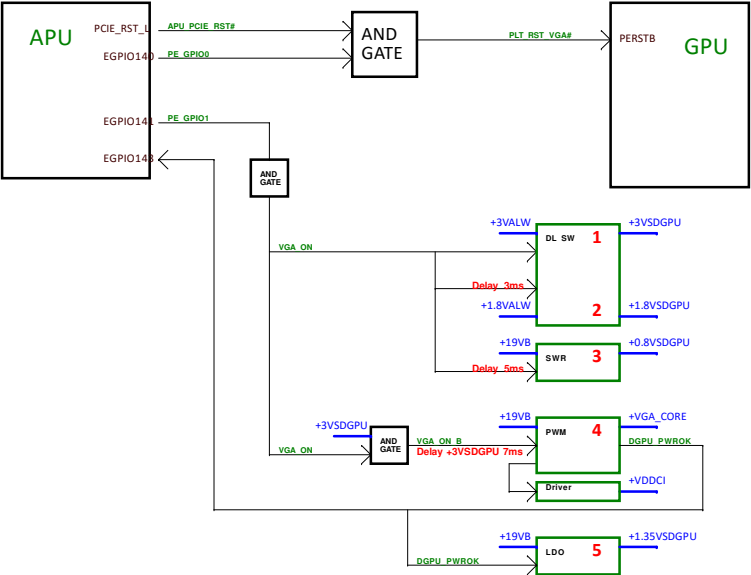
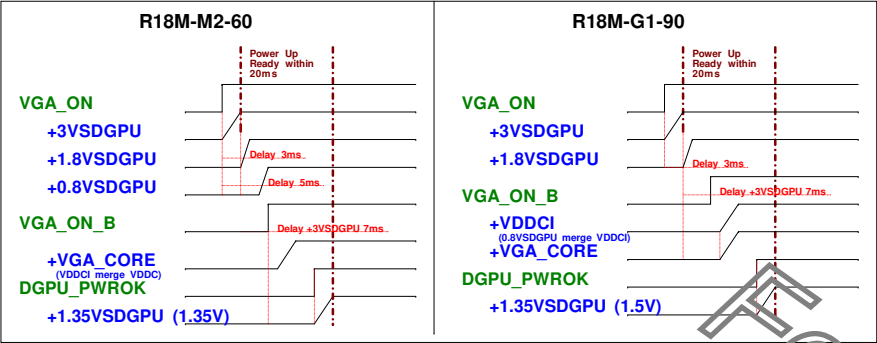
B1 Channel



5.3 Power-up/down Sequence

"R17M-P1-50 / R17M-P1-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/μs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 μs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.



For AMD R17M-P1-50/R18M-M2-60/R18M-G1-90 VRAM

Memory ID/Vendor/Size	Memory PN R3(ABOI) A0	Memory PN R3(ABOI) A1	Memory PN R3(ABOI) B0	Memory PN R3(ABOI) B1
000 (5Gb) SAMSUNG (6Gb) 256M x32	UV1001 V4G_S@ UV1001 PV4G_S@ S IC D5 256M32 K4G80325FB-HC03 FBGA ABOI SA000094R30	UV1002 V4G_S@ UV1002 PV4G_S@ S IC D5 256M32 K4G80325FB-HC03 FBGA ABOI SA000094R30	UV1003 V4G_S@ S IC D5 256M32 K4G80325FB-HC03 FBGA ABOI SA000094R30	UV1004 V4G_S@ S IC D5 256M32 K4G80325FB-HC03 FBGA ABOI SA000094R30
001 (5Gb) HYNIX (6Gb) 256M x32	UV1001 V4G_H@ UV1001 PV4G_H@ S IC D5 256M32 H5GC8H24MJR-T2C BGA ABOI SA000092G20	UV1002 V4G_H@ UV1002 PV4G_H@ S IC D5 256M32 H5GC8H24MJR-T2C BGA ABOI SA000092G20	UV1003 V4G_H@ S IC D5 256M32 H5GC8H24MJR-T2C BGA ABOI SA000092G20	UV1004 V4G_H@ S IC D5 256M32 H5GC8H24MJR-T2C BGA ABOI SA000092G20
010 (5Gb) SAMSUNG 128M x32	UV1001 V2G_S@ UV1001 PV2G_S@ S IC D5 128M32 K4G41325FE-HC28 FBGA ABOI SA000091T30	UV1002 V2G_S@ UV1002 PV2G_S@ S IC D5 128M32 K4G41325FE-HC28 FBGA ABOI SA000091T30	UV1003 V2G_S@ S IC D5 128M32 K4G41325FE-HC28 FBGA ABOI SA000091T30	UV1004 V2G_S@ S IC D5 128M32 K4G41325FE-HC28 FBGA ABOI SA000091T30
011 (5Gb) HYNIX 128M x32	UV1001 V2G_H@ UV1001 PV2G_H@ S IC D5 128M322.5G H5GC4H24AJR-T2C ABOI SA000085V70	UV1002 V2G_H@ UV1002 PV2G_H@ S IC D5 128M322.5G H5GC4H24AJR-T2C ABOI SA000085V70	UV1003 V2G_H@ S IC D5 128M322.5G H5GC4H24AJR-T2C ABOI SA000085V70	UV1004 V2G_H@ S IC D5 128M322.5G H5GC4H24AJR-T2C ABOI SA000085V70
100 (5Gb) MICRON (6Gb) 256M x32	UV1001 V4G_M@ UV1001 PV4G_M@ S IC D5 256M32 MT51J256M32HF-60A ABOI SA000096K30	UV1002 V4G_M@ UV1002 PV4G_M@ S IC D5 256M32 MT51J256M32HF-60A ABOI SA000096K30	UV1003 V4G_M@ S IC D5 256M32 MT51J256M32HF-60A ABOI SA000096K30	UV1004 V4G_M@ S IC D5 256M32 MT51J256M32HF-60A ABOI SA000096K30

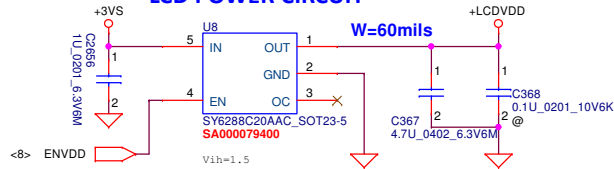
AMD GPU PN

R17M-P1-50 PN R3(ROH)
UV1 RX540@ S IC 216-0905018 A1 R17M-P1-50 ABOI SA0000ALY20
R18M-M2-60 PN R1(ROH)
UV1 RE35@ S IC 216-0915006 A0 R18M-M2-60 FCBGA 769P GPU 0FA SA00008FE00
R18M-G1-90 PN R1(ROH)
UV1 RX565@ S IC 216-0908001 A1 R18M-G1-90 FCBGA 769P GPU 0FA SA00008FF00

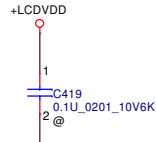
For AMD R18M-G1-90 VRAM Table (7Gb)

Memory ID/Vendor/Size	Memory PN R3(ABOI) A0	Memory PN R3(ABOI) A1	Memory PN R3(ABOI) B0	Memory PN R3(ABOI) B1
000 (7Gb) SAMSUNG (7Gb) 256M x32	UV1001 V4G_S7G@ S IC D5 256M32 K4G80325FB-HC28 FBGA ABOI SA000092D00	UV1002 V4G_S7G@ S IC D5 256M32 K4G80325FB-HC28 FBGA ABOI SA000092D00	UV1003 V4G_S7G@ S IC D5 256M32 K4G80325FB-HC28 FBGA ABOI SA000092D00	UV1004 V4G_S7G@ S IC D5 256M32 K4G80325FB-HC28 FBGA ABOI SA000092D00
001 (7Gb) HYNIX (7Gb) 256M x32	UV1001 V4G_H7G@ S IC D5 256M32 H5GC8H24MJR-R0C BGA ABOI SA00009U110	UV1002 V4G_H7G@ S IC D5 256M32 H5GC8H24MJR-R0C BGA ABOI SA00009U110	UV1003 V4G_H7G@ S IC D5 256M32 H5GC8H24MJR-R0C BGA ABOI SA00009U110	UV1004 V4G_H7G@ S IC D5 256M32 H5GC8H24MJR-R0C BGA ABOI SA00009U110
100 (7Gb) MICRON (7Gb) 256M x32	UV1001 V4G_M7G@ S IC D5 256M32 MT51J256M32HF-70A ABOI SA00009TY10	UV1002 V4G_M7G@ S IC D5 256M32 MT51J256M32HF-70A ABOI SA00009TY10	UV1003 V4G_M7G@ S IC D5 256M32 MT51J256M32HF-70A ABOI SA00009TY10	UV1004 V4G_M7G@ S IC D5 256M32 MT51J256M32HF-70A ABOI SA00009TY10

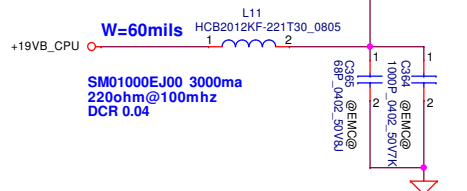
LCD POWER CIRCUIT



Place closed to JEDP1

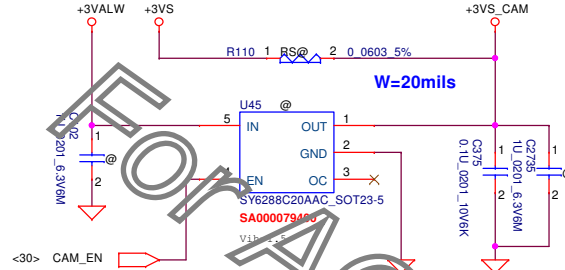
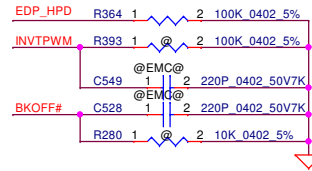
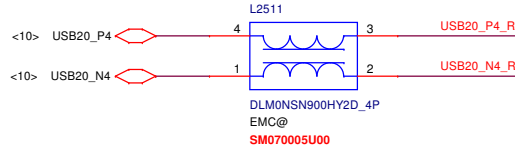


W=60mils



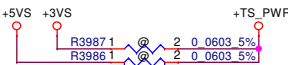
<8>	EDP_TXP0	C371	1	2	.1U	0402	16V7K	EDP_TXP0_C
<8>	EDP_TXN0	C372	1	2	.1U	0402	16V7K	EDP_TXN0_C
<8>	EDP_TXP1	C373	1	2	.1U	0402	16V7K	EDP_TXP1_C
<8>	EDP_TXN1	C374	1	2	.1U	0402	16V7K	EDP_TXN1_C
<8>	EDP_TXP2	C2695	1	2	.1U	0402	16V7K	EDP_TXP2_C
<8>	EDP_TXN2	C2696	1	2	.1U	0402	16V7K	EDP_TXN2_C
<8>	EDP_TXP3	C2698	1	2	.1U	0402	16V7K	EDP_TXP3_C
<8>	EDP_TXN3	C2697	1	2	.1U	0402	16V7K	EDP_TXN3_C

<8>	EDP_AUXP	C370	1	2	.1U	0402	16V7K	EDP_AUXP_C
<8>	EDP_AUXN	C369	1	2	.1U	0402	16V7K	EDP_AUXN_C

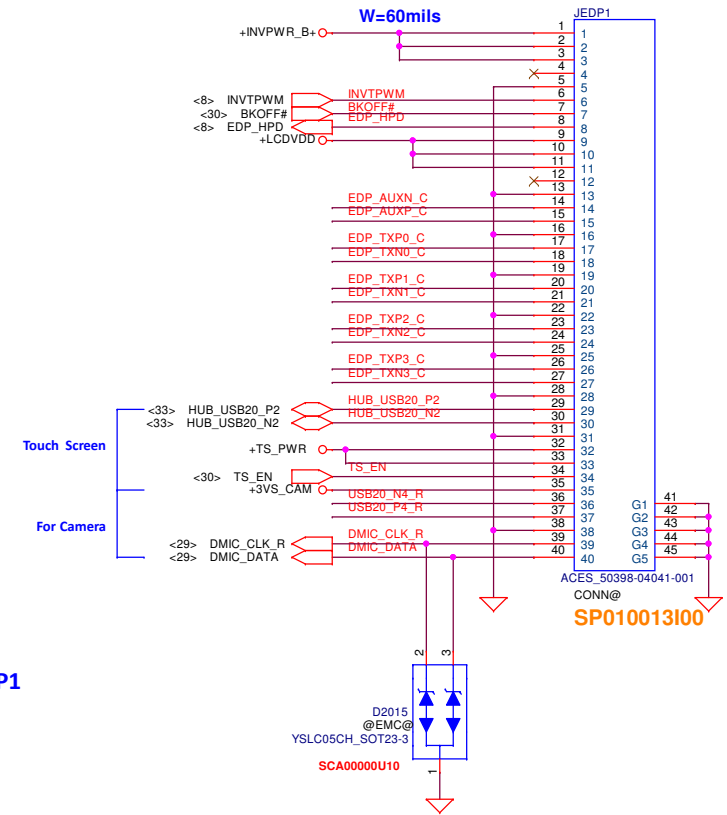


Place closed to JEDP1

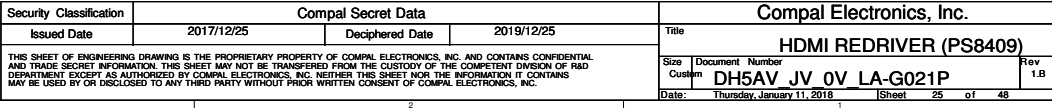
Touch Screen



LED PANEL Conn.





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Size	Document Number	Rev		1.8	
Custom	DH5AV JV 0V LA-G021P				
Date:	Monday, December 25, 2017	Sheet	24	of	48



The schematic shows the routing of the LAN_PWR_EN signal. On the left, a microcontroller pin labeled "LAN_PWR_EN" is connected to a net named "LAN_PWR_EN". This net passes through a capacitor CL14 (1U_0201_63VM) and a resistor RL2 (0.0805_5%) before entering the IN pin of the SA000079400 PHY chip. The PHY chip's OUT pin is connected to another net named "LAN_PWR_EN", which then connects to the LAN_PWR_EN pin of the microcontroller on the right. A third net, labeled "<30>", is also shown connected to the PHY chip's EN pin.

reserve EC_PME# pull high 100K to +3VALV_EC

<30> LAN_WAKE#  RL3 2 RSB 1 0 0402 5%
+3V_LAN_O  RL8 1 2 10K 0402 5%

<10> CLK_PCIE_P4
<10> CLK_PCIE_N4

PU at PCH side

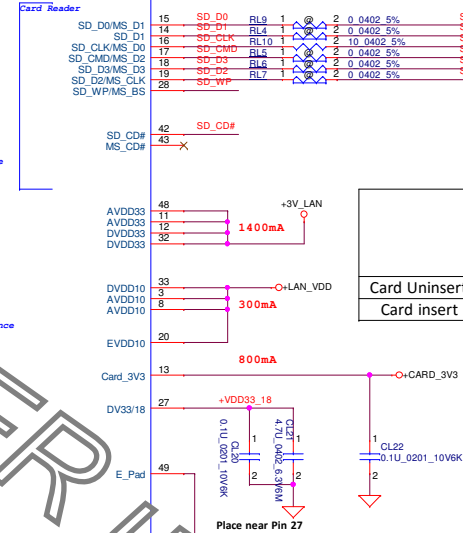
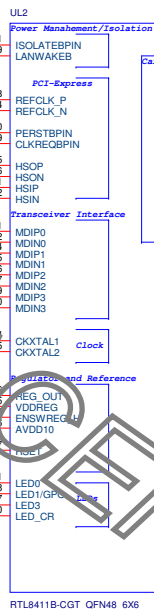
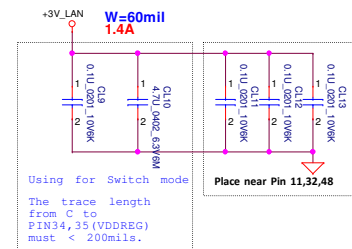
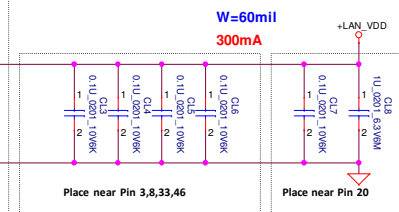
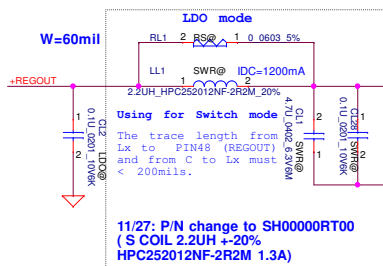
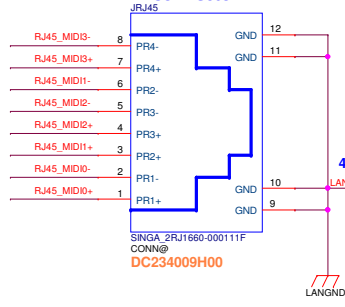
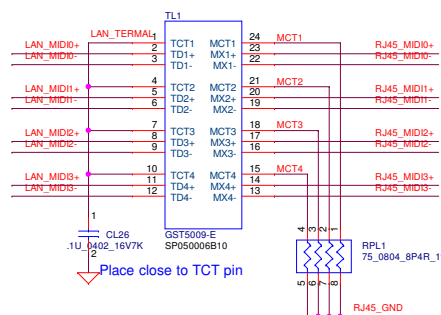
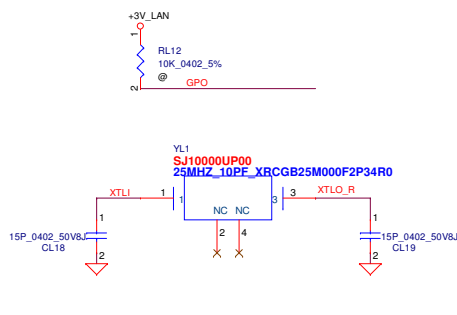
<9.15,27.28>
<10> APU_PCIE_RST#
CLKREQ_PCIE#4

CL15,CL17 close to UL2

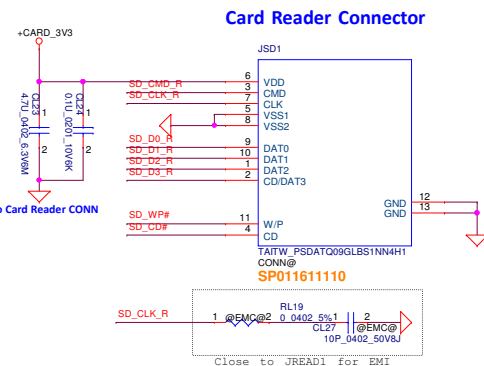
<6> PCIE_ARX_DTX_P4

CL17 1 2 1U 0402 187K
CL15 1 2 1U 0402 187K

CL15,CL17 close to UL2

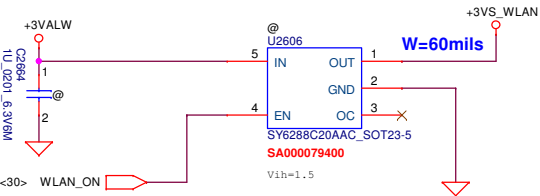
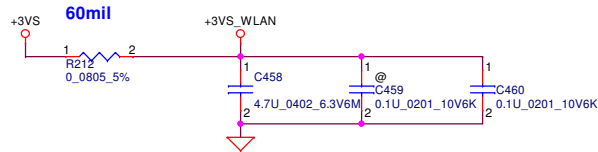


	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Close	Open	Close



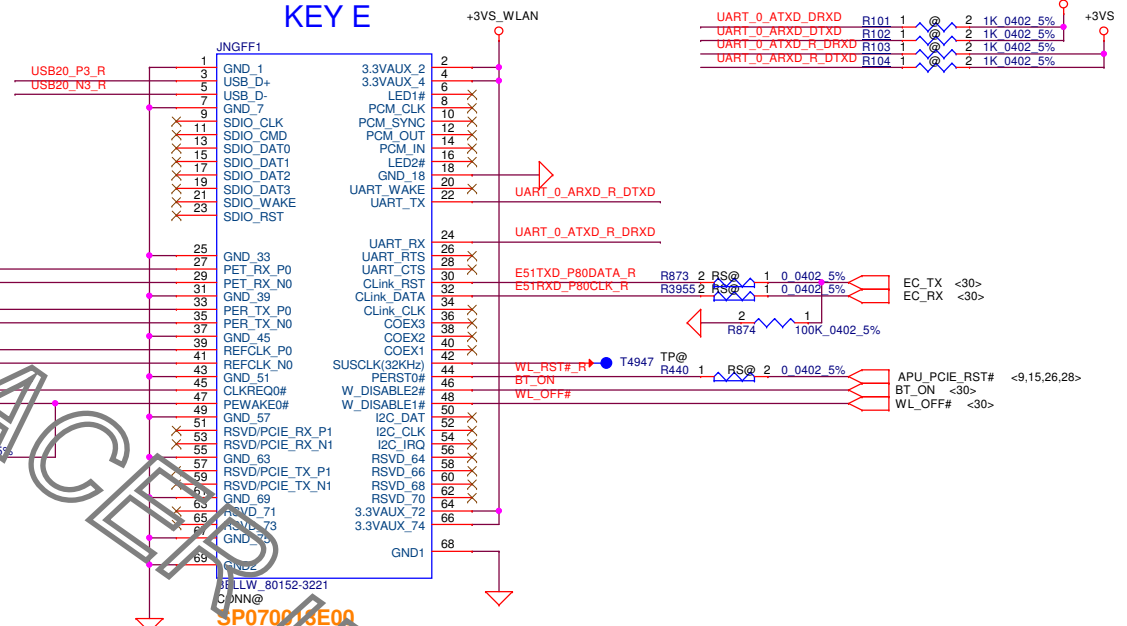
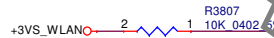
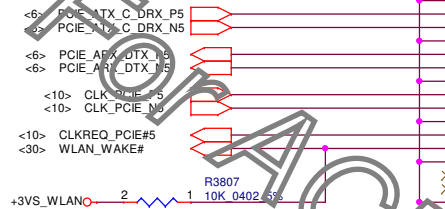
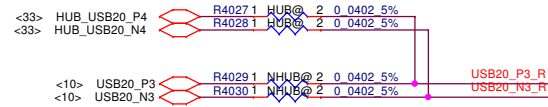
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2017/12/25	Deciphered Date	2019/12/25	Title	LAN RTL8411-CG	
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				Custm	DH5AV_JV_0V LA-G021P	1.B
				Date	Monday, December 25 2017	1 Sheet, 36 of 48

Wireless LAN



NGFF WL+BT (KEY E)

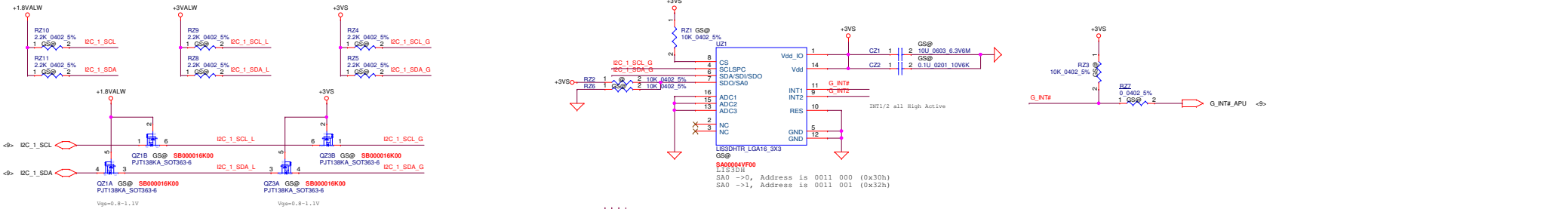
74	1.3v	GND	75
72	1.8v	RESERVED/REFCLKN1	73
70	UM_Power_SNK/GPIO/PWAVE1#	RESERVED/REFCLKP1	71
68	UM_Power_SNK/CLKREQ1#	GND	69
66	UM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I/O)(0.3V)	GND	61
60	QCC CLK (I/O)(0.3V)	Reserved/PETn1	61
58	QCC DATA (I/O)(0.3V)	Reserved/PETp1	59
56	W_DISABLE#1 (O)(0.3V)	GND	57
54	Reserved_W_DISABLE#2 (O)(0.3V)	PWAVE#2 (O)(0.3V)	55
52	PERST0N (O)(0.3V)	CLKREQ#n (O)(0.3V)	53
50	SUSCn(32MHz) (O)(0.3V)	GND	51
48	CODE1 (I/O)(1.8V)	REFCLKN0	49
46	CODE2(O)(0.1.8V)	REFCLKP0	47
44	CODE3(O)(0.1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0.1.8V)	PETn0	37
34	UART CTS (I/O)(1.8V)	PETp0	35
32	UARTTx (O)(0.1.8V)	GND	33
	UART Rx (I/O)(1.8V)	SDIO_RESET# (O)(0.1.8V)	23
22	UART Rx (I/O)(1.8V)	SDIO_Wake# (I)(0.1.8V)	21
20	UART Wake# (I)(0.3V)	SDIO DAT#(O)(0.1.8V)	19
18	GND	SDIO DAT#(I/O)(0.1.8V)	17
16	LED#2 (I)(I/O)	SDIO DAT#2(O)(0.1.8V)	17
14	PCM_OUT/ISD_OUT (O)(0.1.8V)	SDIO DAT#1(I/O)(0.1.8V)	15
12	PCM_IN/ISD_IN (I/O)(1.8V)	SDIO DAT#0(O)(0.1.8V)	13
10	PCM_SYNC/ISD WS (O)(0.1.8V)	SDIO CMD#(O)(0.1.8V)	11
8	PCM_CLK/ISD SCK (O)(0.1.8V)	SDIO CLK#(O)(0.1.8V)	9
6	LED#1 (I)(I/O)	GND	7
4	1.8V	USB_D+	5
2	1.8V	USB_D-	3
	1.8V	GND	1



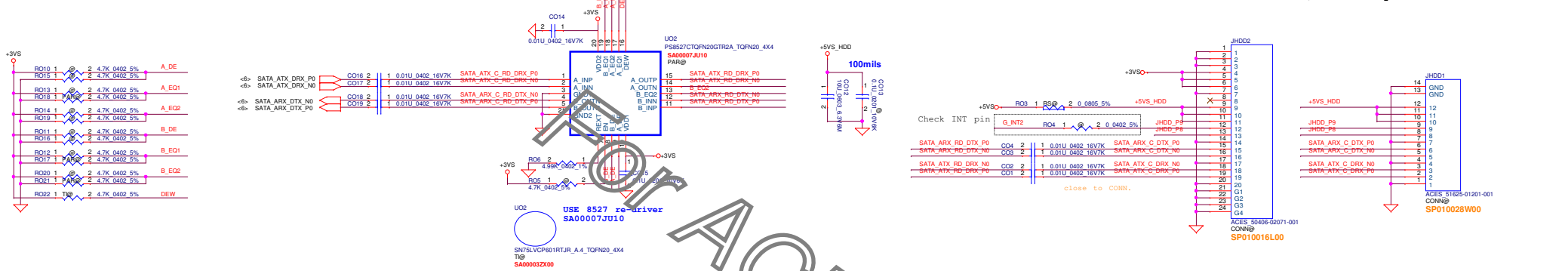
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Issued Date	2017/12/25	Deciphered Date	2019/12/25	Title			
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				Size	Document	Number	Rev
				Custm		DH5AV JV 0V LA-G021P	1.B
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SATA Re-Driver and cable HDD Conn.

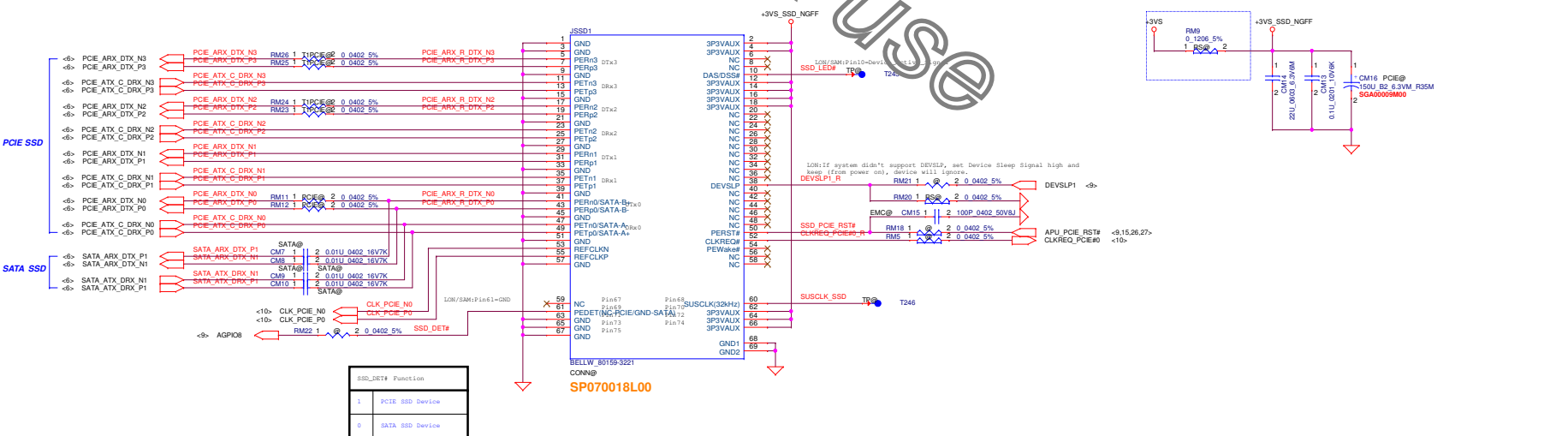
G-Sensor (reserved)



JHDD1, JHDD2Co-Lay



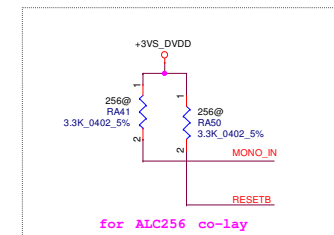
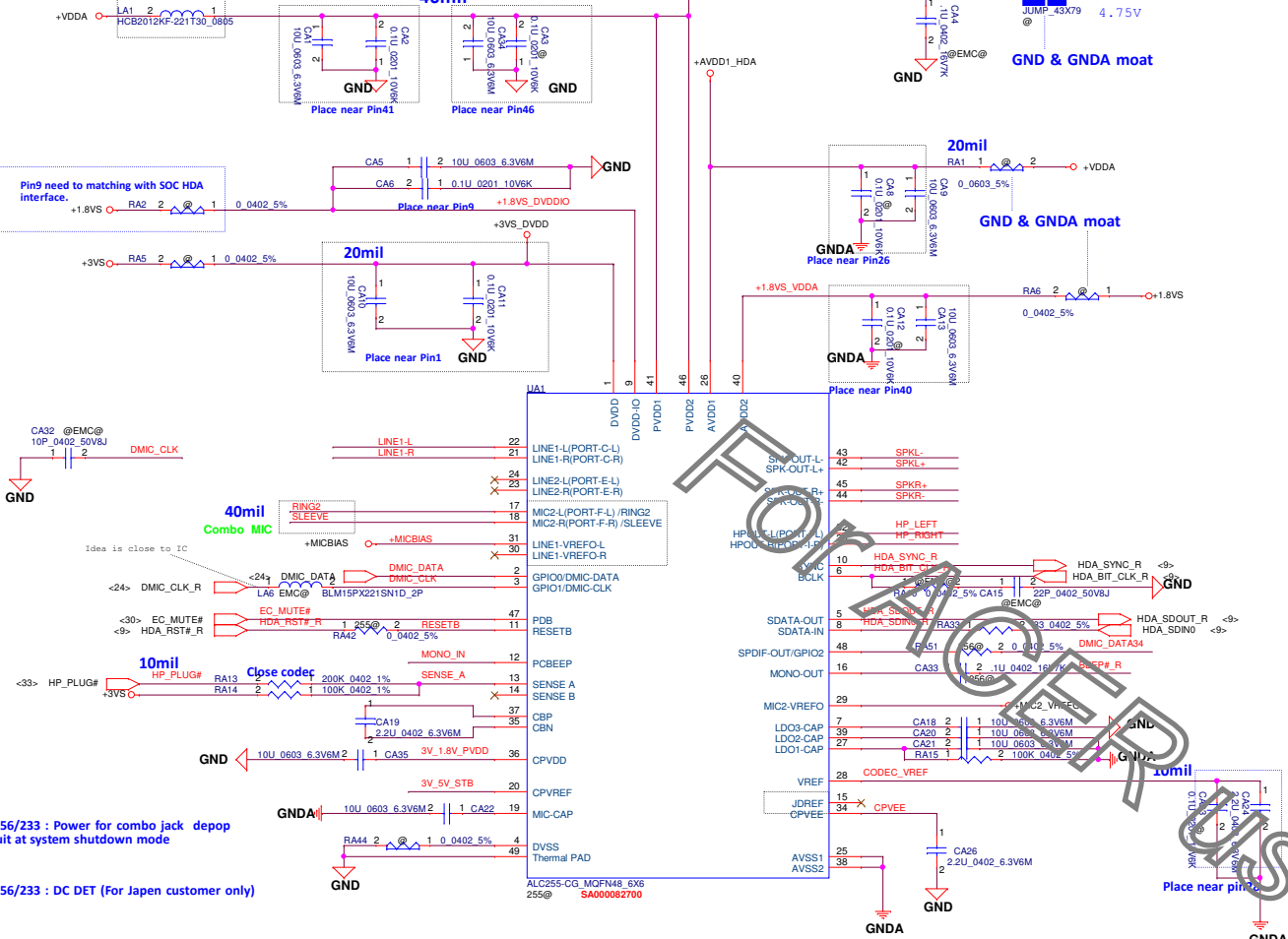
SATA NGFF SSD Conn.



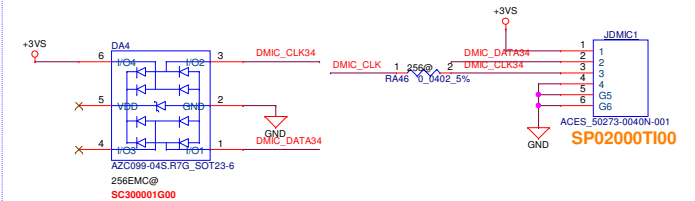
SSD_DET#	Function
PCIE	PCIE SSD Device
SATA	SATA SSD Device

HD Audio Codec

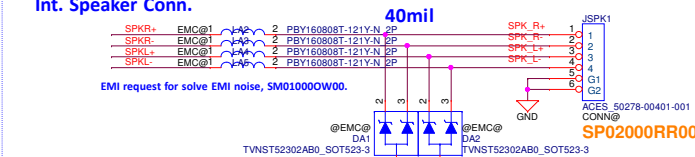
SM01000E100 3000mA 220ohm@100mhz DCR 0.04



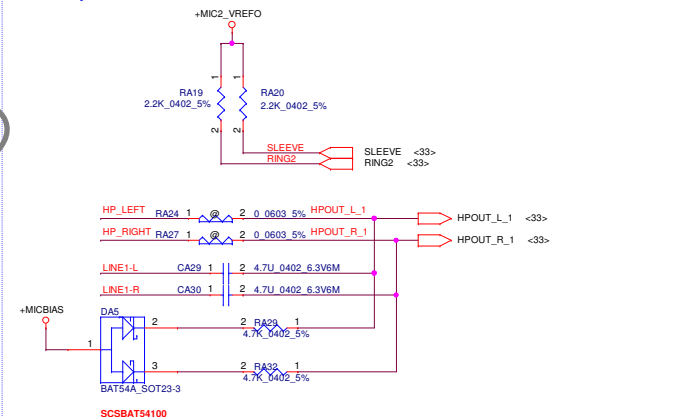
DMIC3/4 Conn. (support on 256)



Int. Speaker Conn.

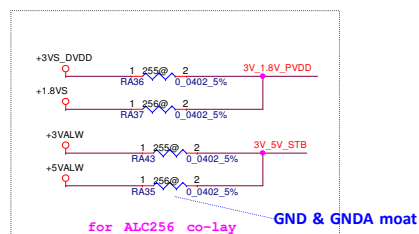
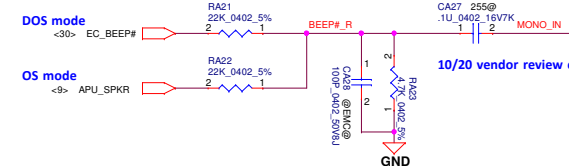


Headphone Out



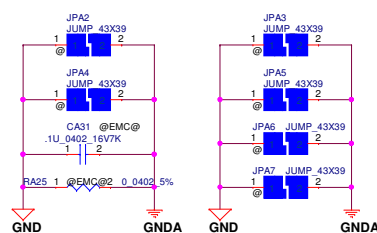
Pin20
ALC255/256/233 : Power for combo jack depop
circuit at system shutdown mode

Pin4
ALC255/256/233 : DC DET (For Japen customer only)



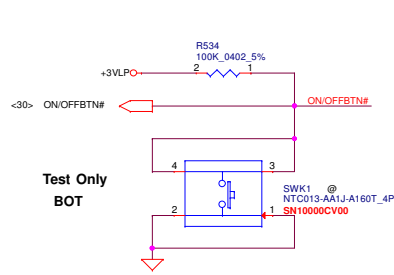
Pin15
ALC255/256/233 : Jack Detect for SPDIF-OUT and SPK-OUT port

GND & GNDA moat

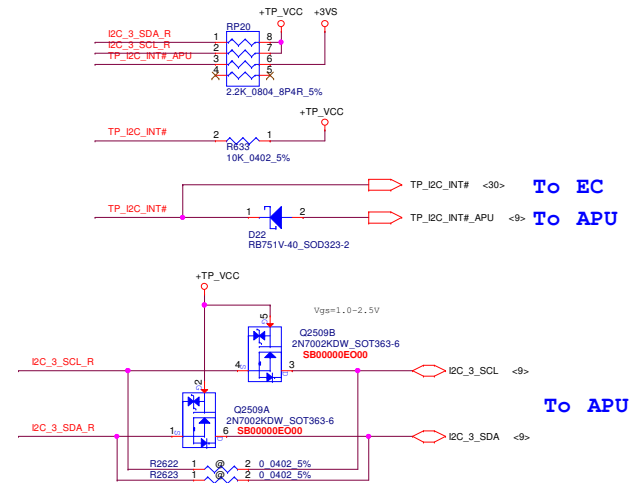
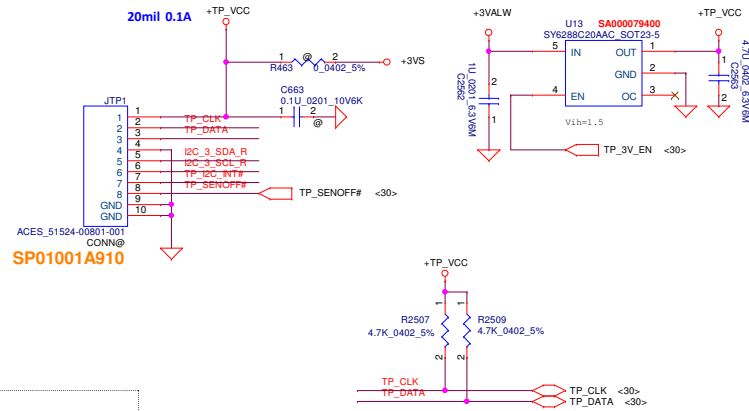


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Customer				DH5AV_JV_0V_LA-G021P
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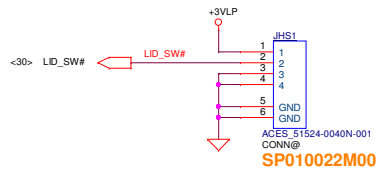
ON/OFF BTN



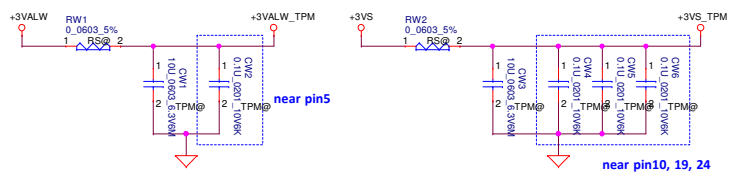
TP/B Conn.



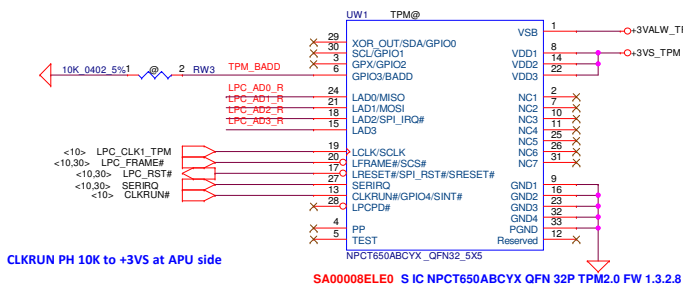
Lid Switch (Hall Effect Switch)



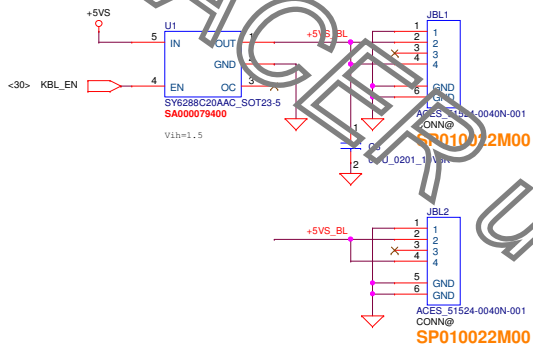
TPM



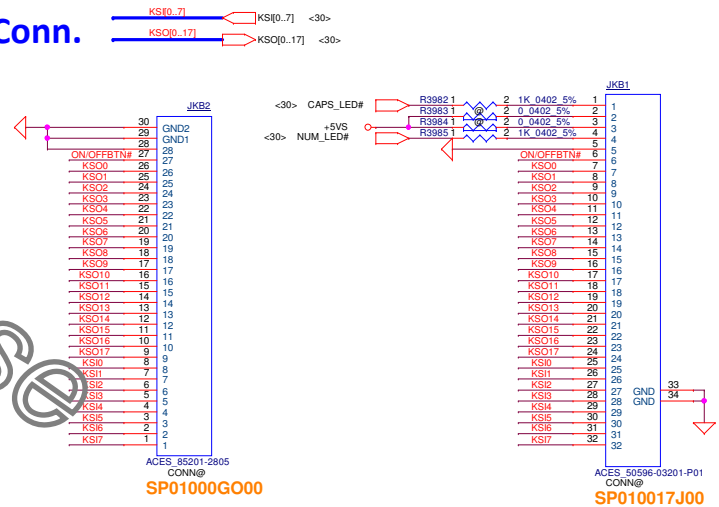
BADD	SELECTION
* 1	AEh(write), AFh(read)



KB BackLight

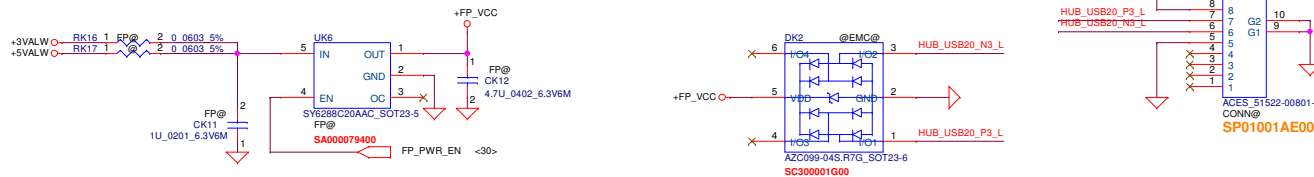


KB Conn.



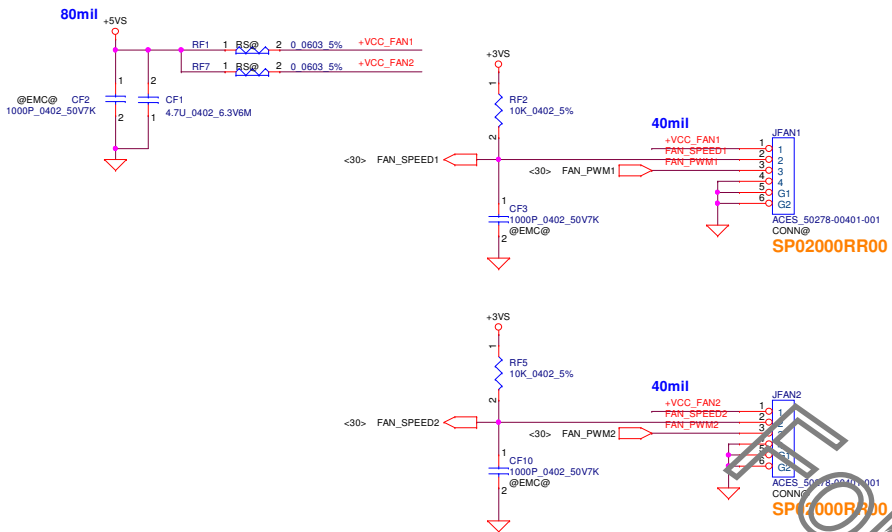
Finger Print

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V

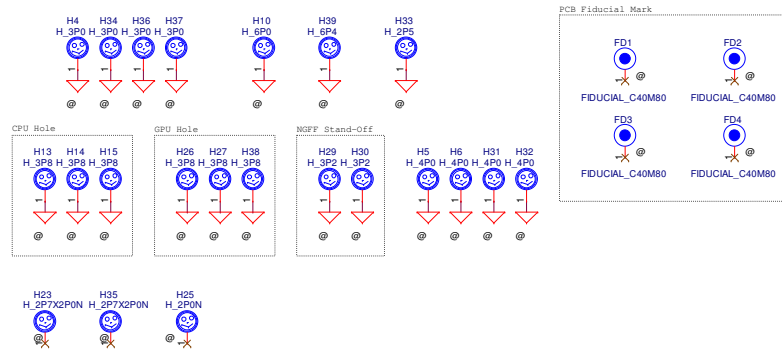


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				Size	Rev
				Document Number Cushman DH5AV JV 0V LA-G021P	
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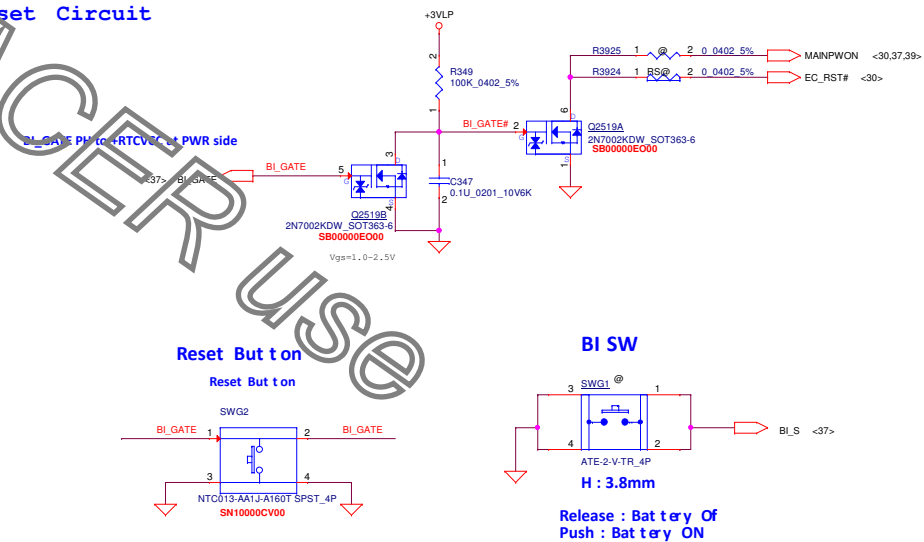
FAN Conn



Screw Hole

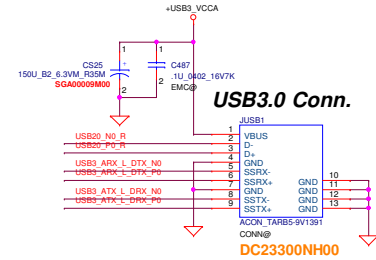
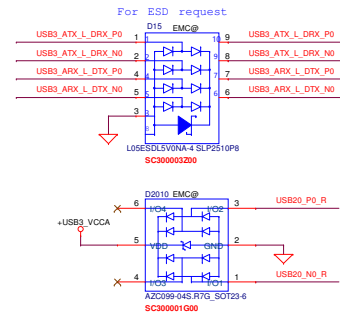
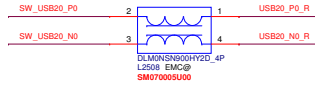


Reset Circuit

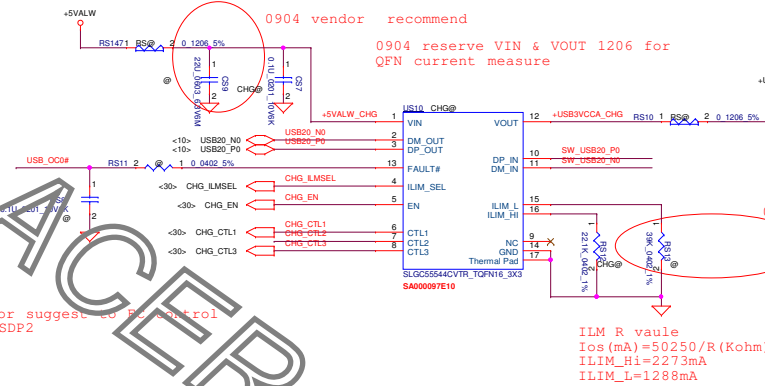
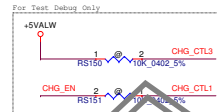
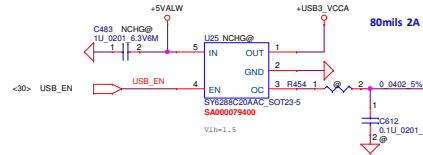


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				FAN/BATT RESET_DEBUG SW			
				Size	Document	Number	Rev
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USB3.0 (Port 0)

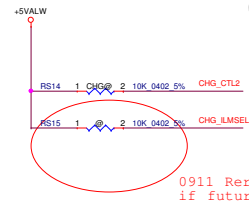


Non-Charger Co-lay

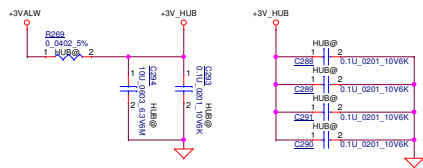


USB Host Charger Truth Table

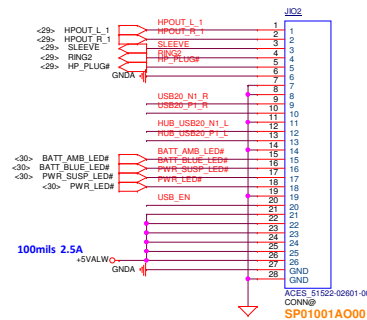
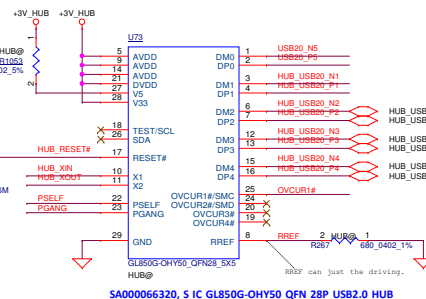
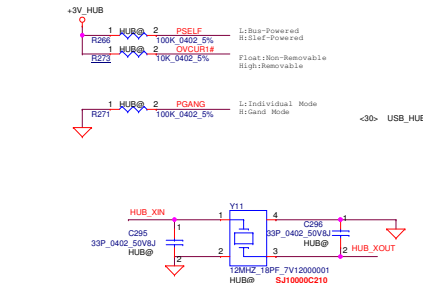
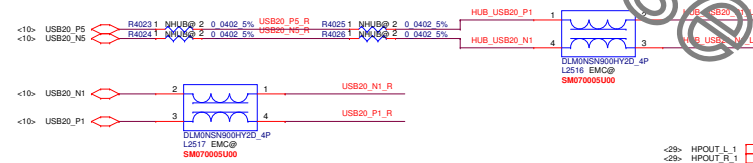
CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
1	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected



0911 Rerserve PU, vendor suggest to EC control
if future need support SDP2

USB HUB

C279 close to U73 pin5
C280 close to U73 pin9
C283 close to U73 pin14
C284 close to U73 pin21

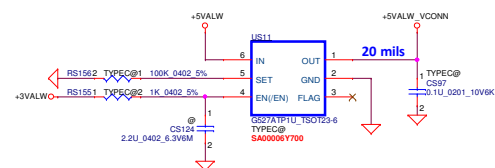


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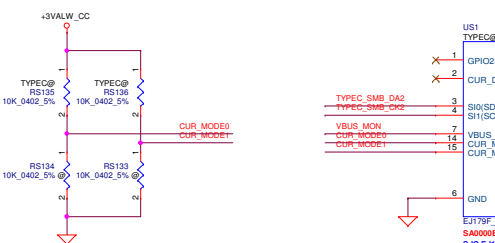
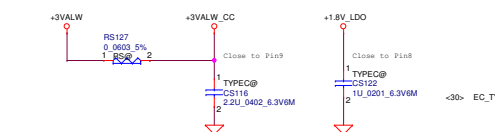
USB3.0 Type-C



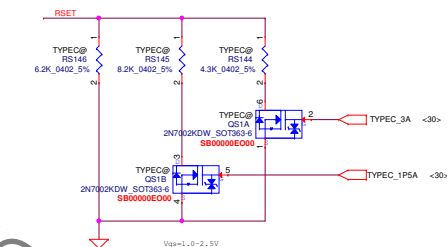
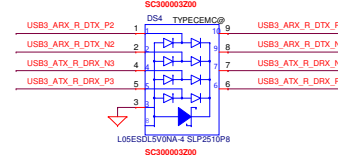
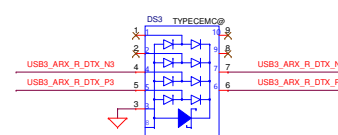
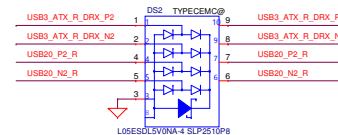
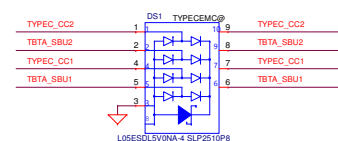
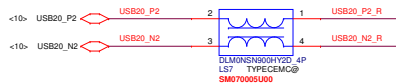
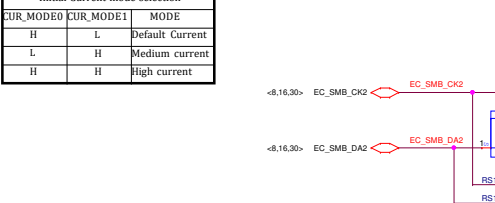
USB3.0 Type-C



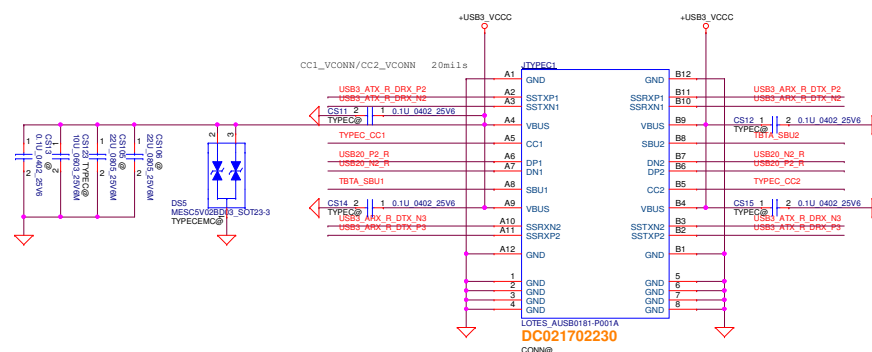
0.2A OCP for VCONN!



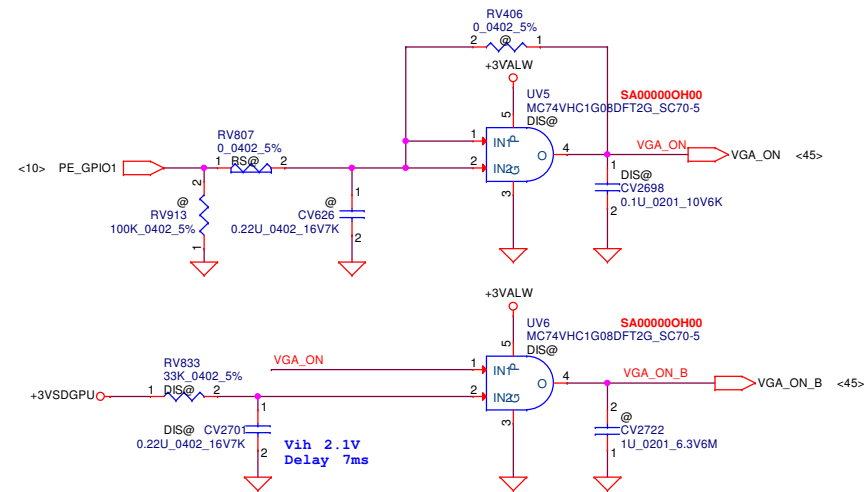
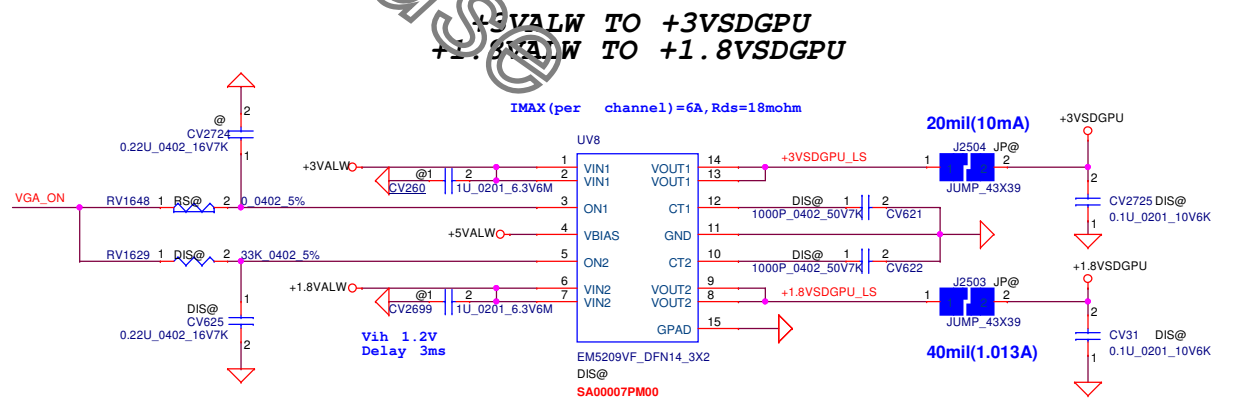
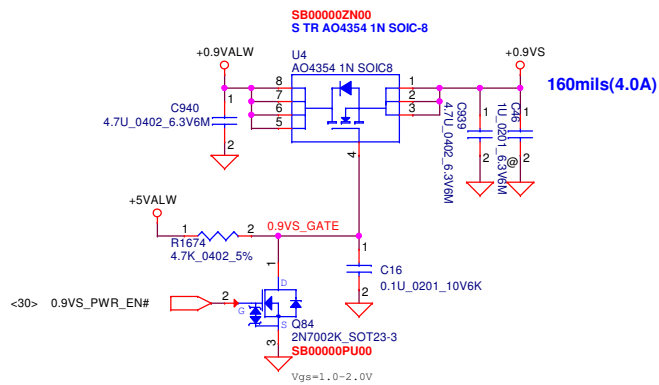
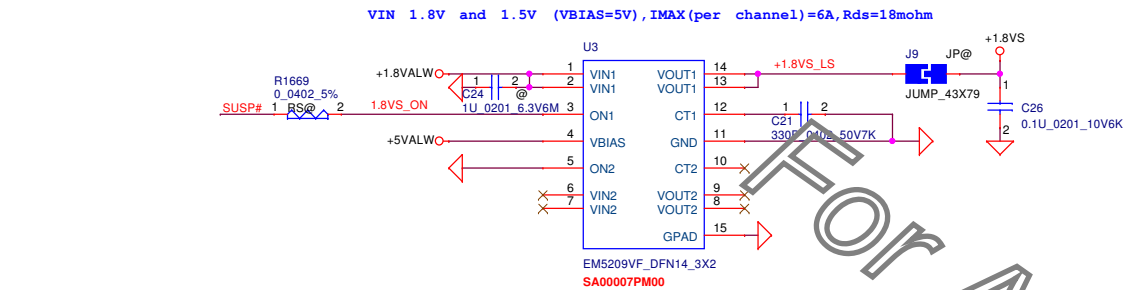
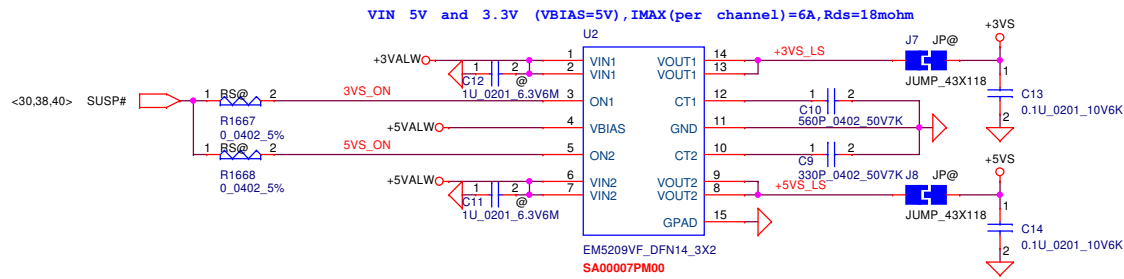
Initial Current mode selection		
CUR_MODE0	CUR_MODE1	MODE
H	L	Default Current
L	H	Medium current
H	H	High current



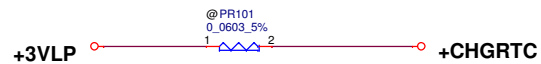
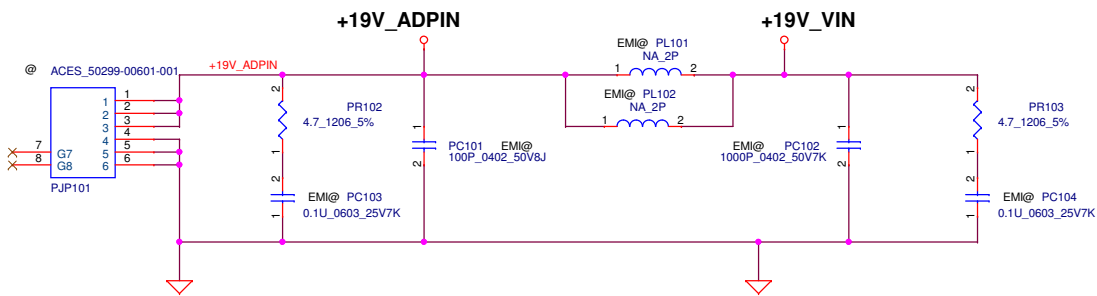
G518 MOS Current Limit				
GPP_B1	GPP_B4	RSET(k Ω)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



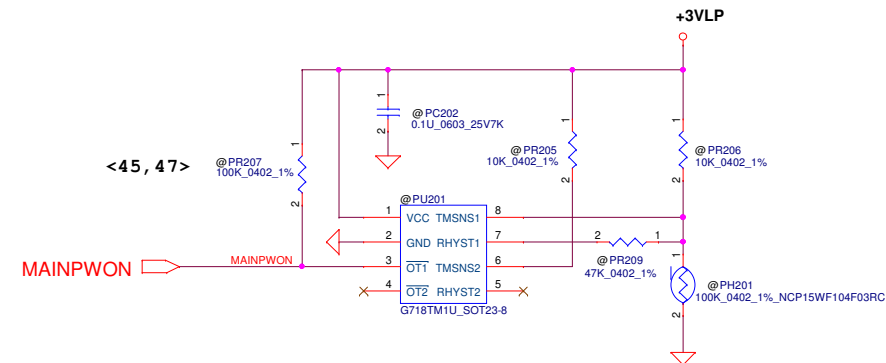
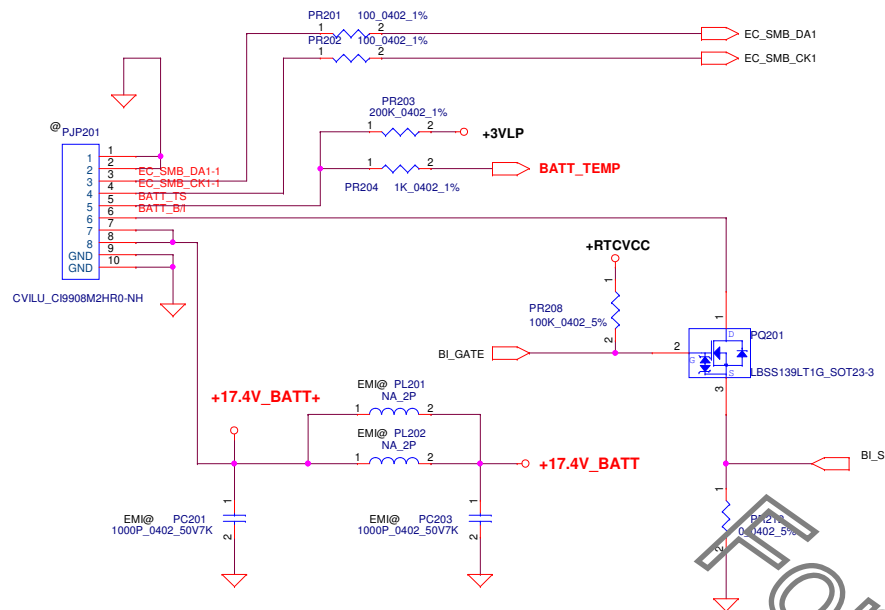
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Size		Document Number			Rev
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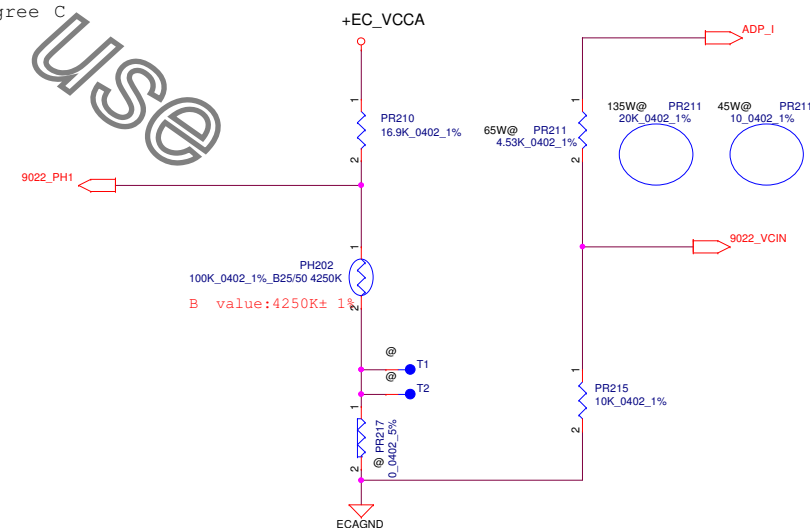
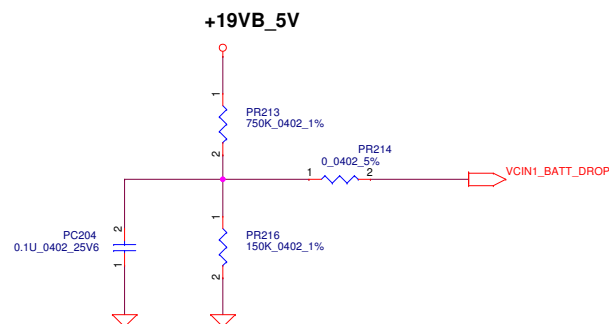
For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92C, 1V	56C, 2V
PH202 (ohm)	7.3092K	26.11K

For KB9012 sense 20mΩ	Active	Recovery
SR 45W	58.5W, 0.61V	58.5W, 0.61V
BR 65W	84.5W, 0.61V	84.5W, 0.61V

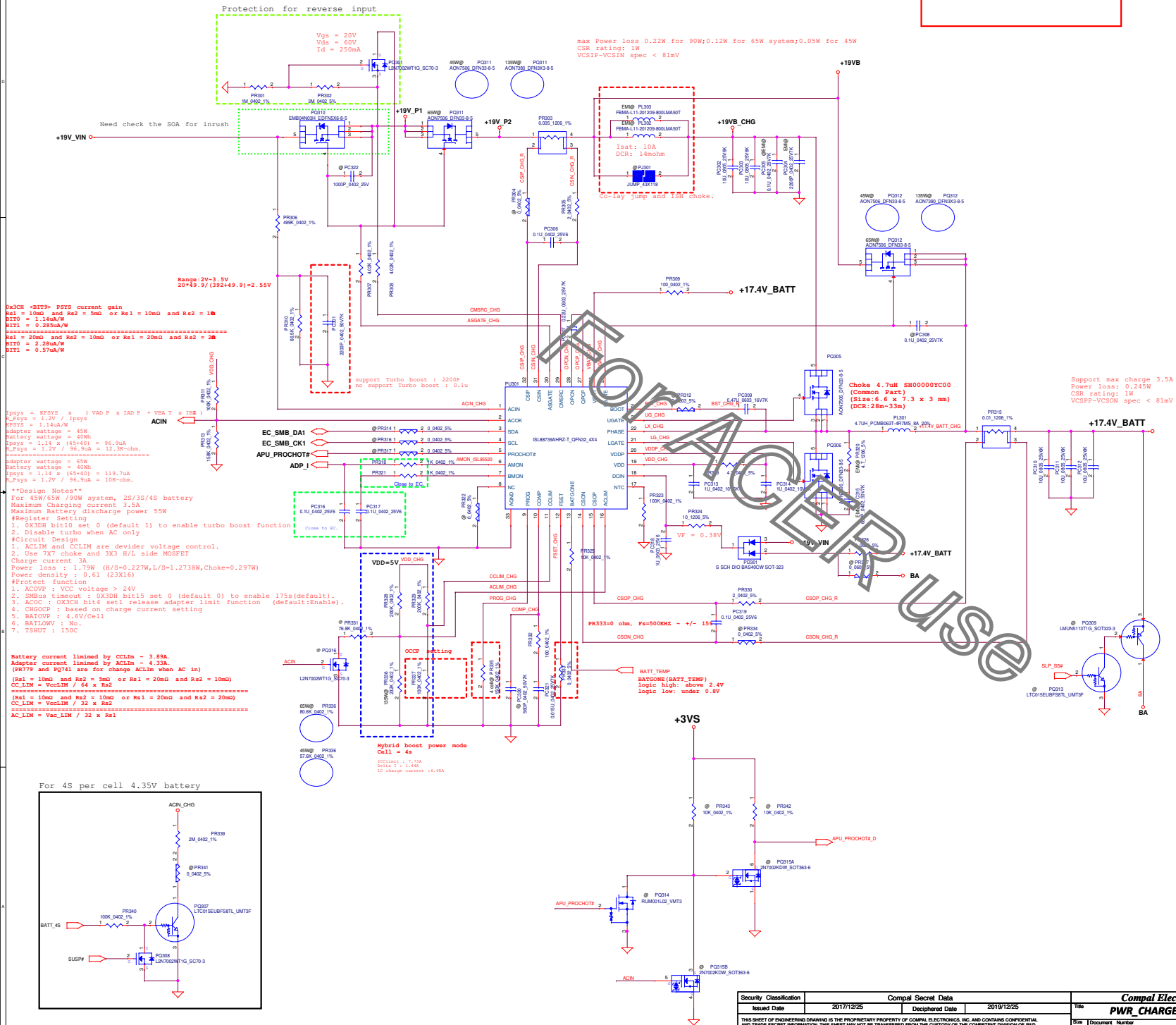
PH202 under CPU bottom side :
CPU thermal protection at 96 degree C (shutdown)
Recovery at 56 degree C

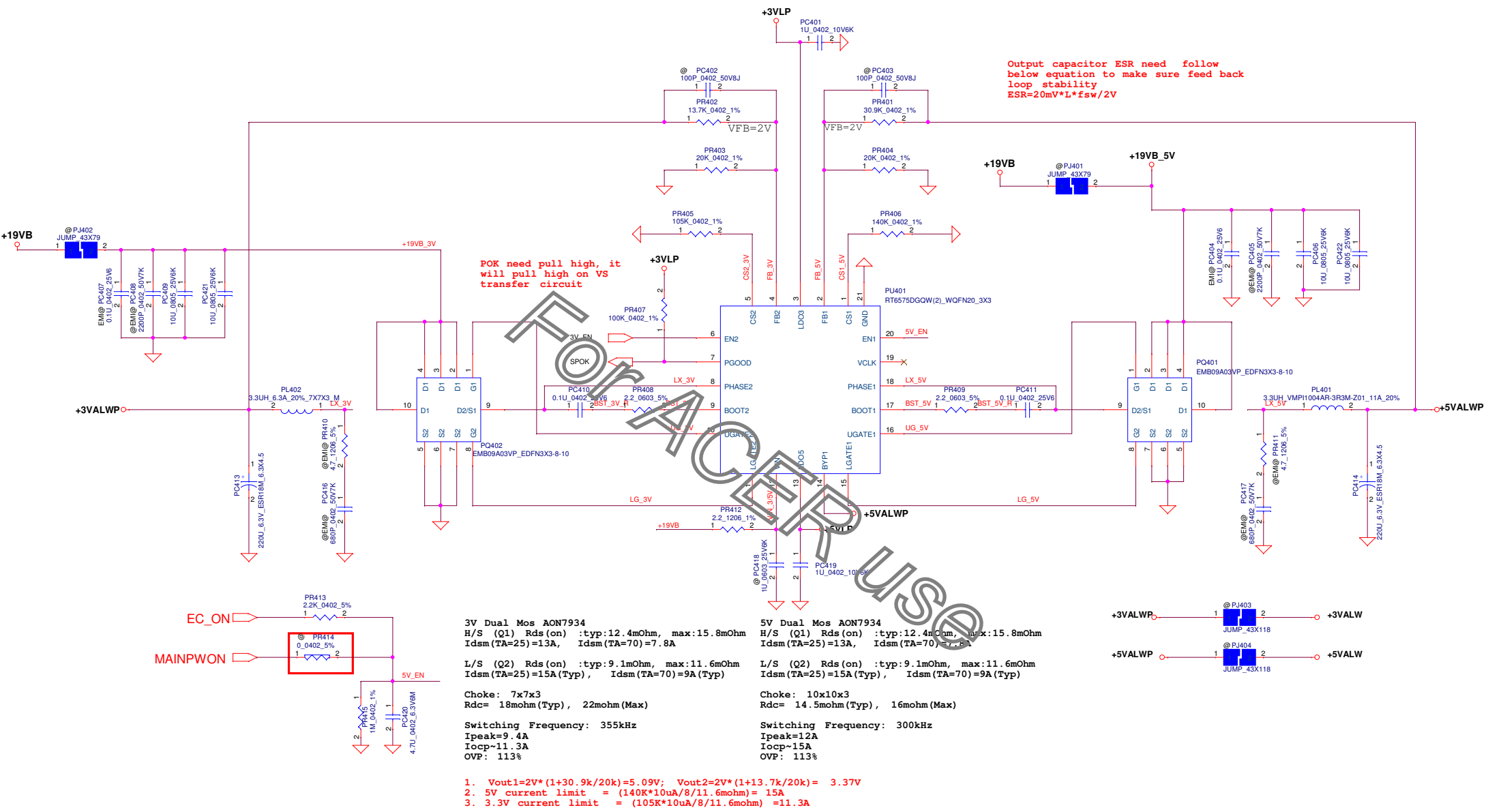
2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design



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								Size	Document Number	Rev
								Custm	DH5AV JV 0V LA-G021P	1.8
Date: Monday, December 25, 2017								Sheet	37	of 48



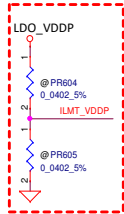


3V Dual Mos AON7934
H/S (Q1) Rds(on) :typ:12.4mOhm, max:15.8mOhm
Idsm(TA=25)=13A, Idsm(TA=70)=7.8A
L/S (Q2) Rds(on) :typ:9.1mOhm, max:11.6mOhm
Idsm(TA=25)=15A(Typ), Idsm(TA=70)=9A(Typ)
Choke: 7x7x3
Rdc= 18mohm(Typ), 22mohm(Max)
Switching Frequency: 355kHz
Ipeak=9.4A
Iocp~11.3A
OVP: 113%

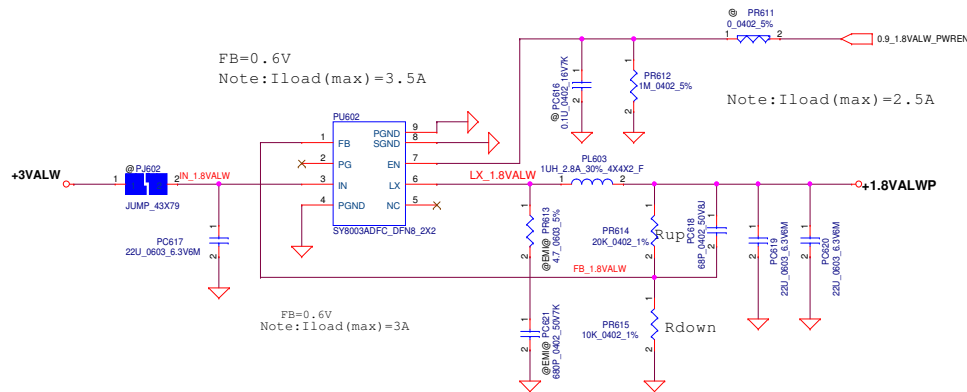
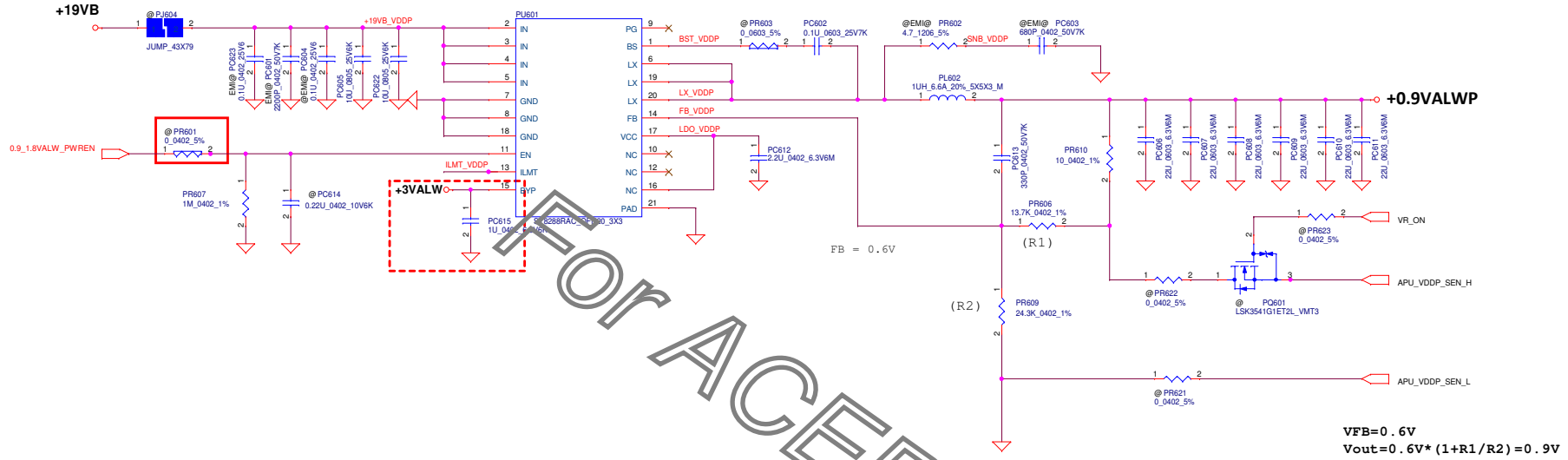
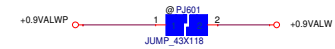
5V Dual Mos AON7934
H/S (Q1) Rds(on) :typ:12.4mOhm, max:15.8mOhm
Idsm(TA=25)=13A, Idsm(TA=70)=7.8A
L/S (Q2) Rds(on) :typ:9.1mOhm, max:11.6mOhm
Idsm(TA=25)=15A(Typ), Idsm(TA=70)=9A(Typ)
Choke: 10x10x3
Rdc= 14.5mohm(Typ), 16mohm(Max)
Switching Frequency: 300kHz
Ipeak=12A
Iocp~15A
OVP: 113%

1. $V_{out1}=2V*(1+30.9k/20k)=5.09V$; $V_{out2}=2V*(1+13.7k/20k)= 3.37V$
2. 5V current limit = $(140K*10uA/8/11.6mohm)= 15A$
3. 3.3V current limit = $(105K*10uA/8/11.6mohm)=11.3A$

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Customer	Document Number	Revision		Date	
	DH5AV_JV_0V_LA-G021P	1.8		Monday, December 25, 2017	
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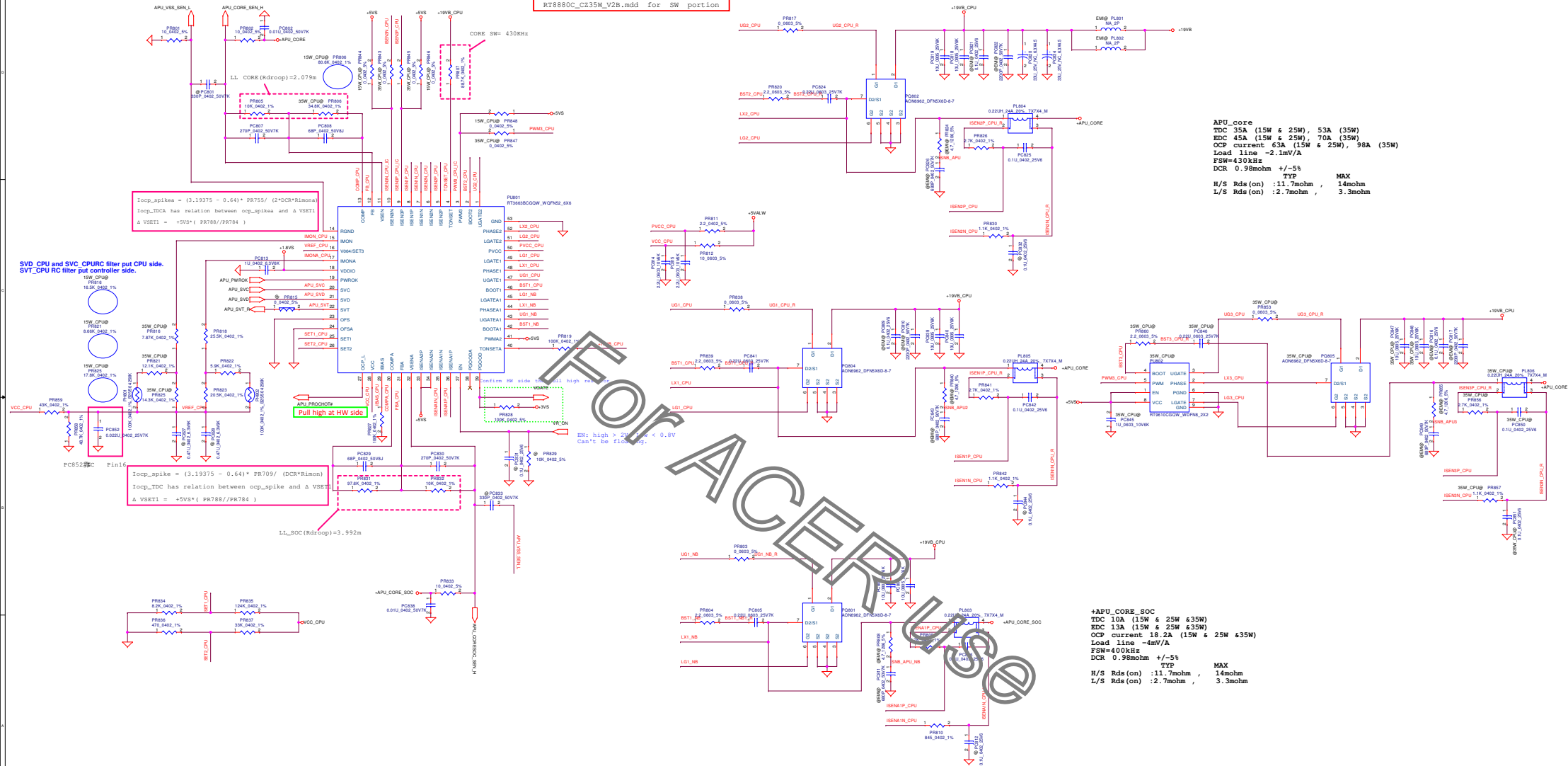
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2




Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

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Size	C	Document Number	DH5AV_JV_0V_LA-G021P	Rev
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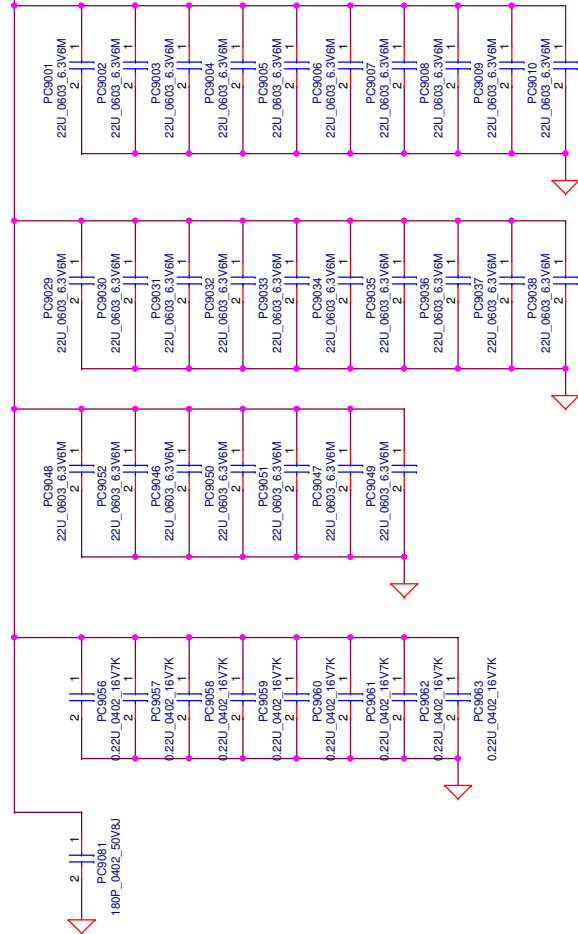
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Module model information
RT8880C_CZ35W_V2A.mdd for IC portion
RT8880C_CZ35W_V2B.mdd for SW portion
```



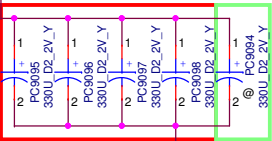
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Issued Date	2017/1/2/25	Deciphered Date	2019/12/25	
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			Item Document Number	1.0
			Date December 25, 2017	Sheet 42 of 48

+APU_CORE

+APU_CORE



+APU_CORE



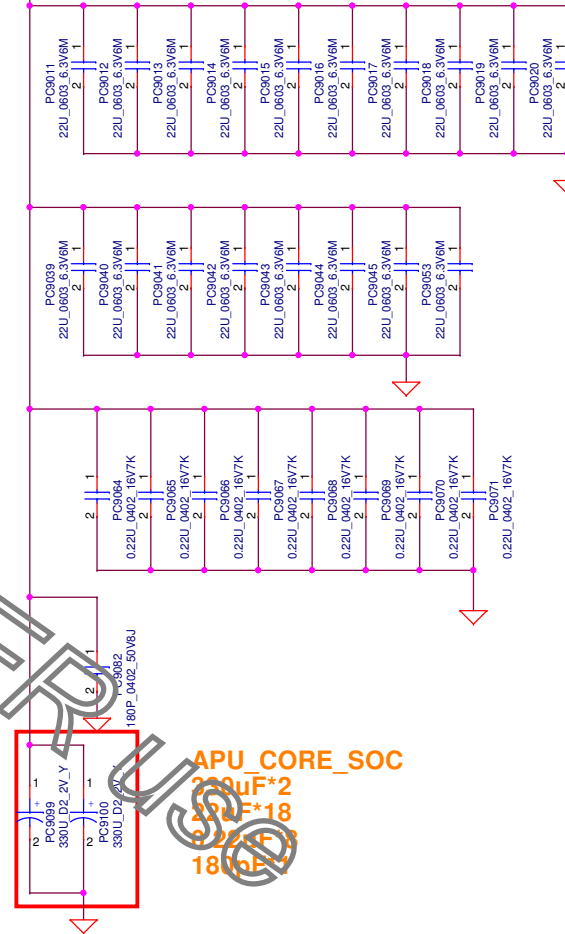
near CPU CPU back side

330u is common part SGA00009S00

APU_CORE
330uF*5
22uF*27
0.22uF*8
180pF*1

+APU_CORE_SOC

+APU_CORE_SOC



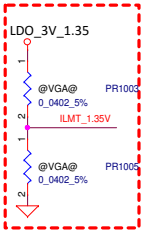
near CPU

330u is common part SGA00009S00

APU_CORE_SOC
330uF*2
22uF*18
0.22uF*8
180pF*1

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				Document Number	1.8
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				Sheet	43 of 48

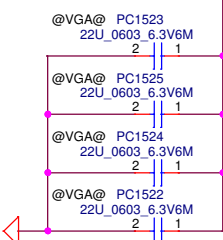
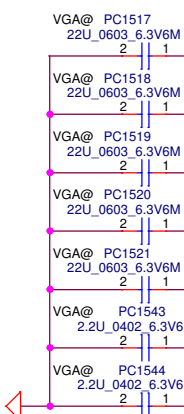
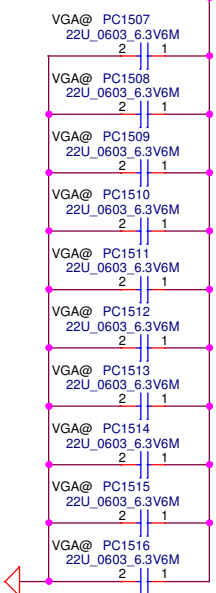
Module model information
SY8208D_V1.mdd



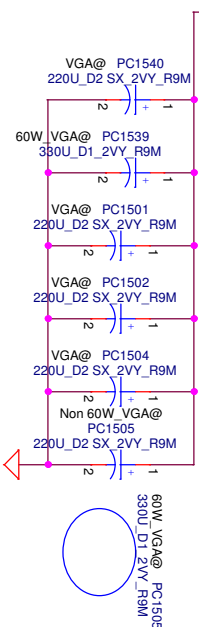
Security Classification	2017/12/25	2017/12/25
Issued Date	2017/12/25	2017/12/25
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				Cuskm	DH5AV_JV_0V_LA-G021P	1.B
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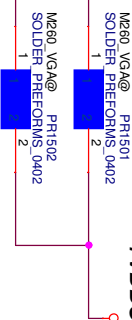
+VGA_CORE



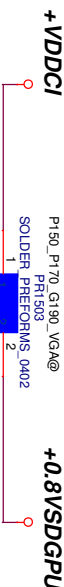
+VGA_CORE



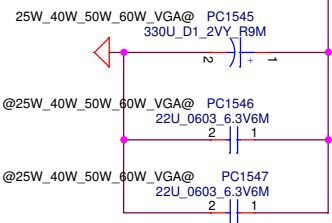
+VGA_CORE



+VDDCI



+0.8VSDGPU



For ACER use

Title		<Title>	
Size	Document Number	Rev	
B	DH9AV_JV_0V_LA-0021P	1.0	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	Down Size for EMI Cap	1.0	39, 41, 42, 44, 45	Change PC315, PC603, PC811, PC826, PC843, PC849, PC1408, PC1426, PC1467, PC1004, PC1442, PC1481 from 680P_50V_K_X7R_0603 (SE025681K80) to 680P_50V_K_X7R_0402 (SE074681K80).	2017/10/20	B
02	Design Update	Down Size for VGA Cap	1.0	45	Change PC1443 from 0.047U_0603_25V7M (SE042473M80) to 0.047U_0402_25V7K (SE00000MJ00)	2017/10/20	B
03	Design Update	Solution Change	1.0	38	Change PQ310 from AON6366E (SB00001D800) to EMB04N03H (SB00001C500) Change 135W Adapter PQ311, PC312 from AON7506 (SB000010A00) to AON7380 SB00001GM00) Delete the PC323 10U_0805_25V (SE00000QK00)	2017/10/20	B
04	Design Update	Down Size for EMI Cap	1.0	36	Change PC101 from 100P_50V_J_NPO_0603 (SE024101J80) to 100P_50V_J_NPO_0402 (SE071101J80). Change PC102 from 1000P_50V_K_X7R_0603 (SE025102K80) to 1000P_50V_K_X7R_0402 (SE074102K80).	2017/10/20	B
05	Design Update	change to r-short	1.0	38, 39, 40, 41, 42	Change PR304, PR314, PR316, PR317, PR322, PR334, PR509, PR510, PR515, PR414, PR611, PR815 (0402) AND PR327, PR312 (0603) 0ohm to r-short	2017/11/1	B
06	Design Update	change HW sequence disable VDDCI	1.0	45	Change PC1476 from 0.22U_0402_10V6K (SE095224K00) to 0.47U_0402_6.3V6K (SE124474K80) Add PR1466 for disable VDDCI when ues R535 GPU	2017/11/1	B
07	Design Update	tune CPU transient and load line	1.0	42	Change PR809 from 2.49K_0402_1% (SD034249180) to 2.7K_0402_1% (SD034270180) Change PR826, PR841, PR856 from 2.26K_0603_1% (SD014226180) to 2.7K_0402_1% (SD034270180) Change PR806 from 53.6K_0402_1% (SD034536280) to 80.6K_0402_1% (SD034806280) 15W CPU Change PC807, PC830 from 330P_0402_50V8J (SE000006I80) to 270P_0402_50V7K (SE074271K80) Change PR859 from 18.2K_0402_1%(SD034182280) to 43K_0402_1% (SD034430280) Change PR858 from 30.9K_0402_1% (SD034309280) to 48.7K_0402_1% (SD034487280) Change PC828 to un pop	2017/11/6	B
08	Design Update	Down Size for EMI Cap	1.0	37	Change PC201, PC203 from 1000P_50V_K_X7R_0603 (SE025102K80) to 1000P_50V_K_X7R_0402 (SE074102K80)	2017/11/14	B
09	Design Update	Down Size for Cap	1.0	40, 39	Change PC507, PC506 from 10U_0805_6.3V6K (SE095216K80) to 10U_0603_6.3V6M (SE000005T80) Change PC416, PC417 from 680P_0603_50V_K_X7R_0603 (SE024681K80) to 680P_0402_50V7K (SE074681K80)	2017/11/14	B
10	Design Update	Cap shortage	1.0	38, 45	Change PC313, PC314, PC1428, PC1429 from 1U_0402_16V6K (SE00000QL00) to 1U_0402_10V6K (SE00000QL10)	2017/11/14	B
11	Design Update	Cap shortage	1.0	44, 46	Change PC1015, PC1476, PC9056, PC9057, PC9058, PC9059, PC9060, PC9061, PC9062, PC9063, PC9064, PC9065, PC9066, PC9067, PC9068, PC9069, PC9070, PC9071 from 0.22U_0402_10V6K (SE095224K00) to 0.22U_0402_16V7K (SE00000R700)	2017/11/14	B
12	Design Update	紅丹測試	1.0	46	Delete PC1538 330U_D1_2VY_R9M (SGA00009S00) Reserved 22U_0603_6.3V6M*4 (SE00000M000) Change PC1505 from 220U_D2 SX_2VY_R9M (SGA20221D40) to 330U_D1_2VY_R9M (SGA00009S00) for CPU VGA	2017/11/14	B
13	Design Update	change to common part	1.0	42	Change PC820, PC834 from 33U_25V_NC_6.3X4.5 (SF000007700) to 33U_25V_NC_6.3X4.5 (SF000007200)	2017/11/14	B
14	Design Update	For sourcer request	1.0	42	Change PC820, PC834 from 33U_25V_NC_6.3X4.5 (SF000007200) to 33U_25V_NC_6.3X4.5 (SF000007700)	2017/11/23	B
15	Design Update	tune VDDP in AMD spec	1.0	41	Change PR609 from 26.7K_0402_1% (SD034267280) to 24.3K_0402_1% (SD00000AT80) PQ601 unpop	2017/11/23	B
16	Design Update	use SW solution in standby mode	1.0	38, 43	PR326 0_0603_5% pop PQ309 LMUN5113T1G_SOT323-3 un pop PQ313 LTC015EUBFS8TL_UMT3F un pop PC9094 330U_D2_2V_Y un pop	2017/11/23	B
17	Design Update	電壓設計 two cell low batt protect	1.0	37	pop PR212 0_0402_5% (SD028000080) pop PC204 0.1U 25V K X5R (SE00000G880) pop PR213 750K +-1% 0402 (SD00000AL80) pop PR214 0 +-5% 0402 (SD028000080) pop PR216 150K +-1% 0402 (SD034150380) pop PR212 0 +-5% 0402 (SD028000080)	2017/11/23	B
18	Design Update	change PQ307 and PQ313 source for source request	1.0	38	change PQ307 & PQ313 form LTC015EUBFS8TL (SB00000RM00) to LMUN5236T1G (SB000011K00)	2017/11/23	B
19	Design Update	adaject BATGONE Threshold	1.0	37	change PR203 from 6.49K_0402_1% (SD034649180) to 200K_0402_1% (SD034200380)	2017/11/23	B
20	Design Update	adaject boost ability	1.0	38	change PC309 from 0.22U_0603_25V7K (SE000005Z80)to 0.47U_0603_16V7K (SE026474K80)	2017/11/23	B
21	Design Update	for EMI request	1.0	38	add PL302/PL303 FBMA-L11-201209-800LMA50T (SM01000U600)	2017/12/22	B
22	Design Update	for ACIN point	1.0	38	change PR306 392K_0402_1% (SD034392380) to 499K_0402_1% (SD034499380) change PR310 49.9K_0402_1% (SD034499280) to 66.5K_0402_1% (SD034665280)	2017/12/22	B

Item	Page#	Date	Request Owner	Issue Description	Solution Description	Rev.
1		07/31		1. Initial		0.1
2		09/30		EVT Final		0.1
3		11/02		1. UW1 change PN(SA00008ELE0) 2. US11,U74 change PN(SA00004ZA00) 3. L43,L44 change PN(SM01000K500) 4. US10 Pin2,3 swap Pin 10,11 (USB Charger modify) 5. RC6155 change location to CLRP1 6. RM23,RM24,RM25,RM26 add 0-ohm with T1PCIE@ 7. All 1uF_0402 capacitor change to 1uF_0201 (SE00000UC00) 8. CS123 change PN(SE00000X200) 9. CC16 change to 1uF (SE00000UC00) 10.RO18 change to pop with PAR@ 11.JDMIC1 change to 4pin connector (SP02000TI00) 12.R1562 pop, R1564 change to 20k (SD034200280) 13.R3_APU change PN(SA0000BBJ20) 14.US12 update value and part description 15.Q101,R101,R102,R103,R104 add with @ for UART0 debug 16.L2508,L2511,LS7 change to small size (SM070005U00) 17.PCB change PN(DAZ28Z00100) 18.SKU_ID change to AGPIO23, AGPIO40 will left N.C. 19.RC30,RC700,RC690,RC1676,RC1677,RC1672,RL1,RL13,RM20,RS10,RS127,RS147,RV807,RV1542,RV1632,R110,R4018 change to R-short 20.UV4 change PN(SA0000A4K00)		1.0
4		11/07		1. CV450,CV451 change to 10pF 2. C796,C797 change to 3.9pF 3. Combine power 11/06 4. R756,R765,R769,R779,R781,R782,R793,R794 change to R-short 5. L2516,L2517 add with EMC@ R4031,R4032 remove 6. RS150,RS151 add with @ for debug		1.0
5		11/15		1. CC120 change to 0402_50V7K (SE074661K80) 2. Combine power		1.0
6		11/20		1. Board ID set by project 2. VRAM table add MICRON VRAM 3. Memory strap pin add MICRON config PV4G_M@ 4. EVT@ change to @ 5. R3APU@ seperate to R3APUDC@ and R3APUQC@ 6. CS11,CS12,CS14,CS15 change to 0.1uF_0402_25V (SE00000G880) 7. TPM@,FP@,GS@,HDT@ remove from BOM PVT Final		1.0
7		12/18		1. C796,C797 change PN to SE07139AC80 (S CER CAP 3.9P 50V C NPO 0402) 2. RW5,RW6,RW7,RW8 change to pop 3. RC6175,RC6174 change to @, RC693 change to DIS@, RC692 change to UMA@ 4. VRAM config V4G_S7G@,V4G_H7G@,V4G_M7G@ add into table and strap-pin 5. RC6175 change to @, RC6174 change to @ 6. US11 change to Power Switch (SA00006Y700, S IC G527ATP1U TSOT-23 6P PW SW) 7. RS154,RS155,RS156 add with TYPEC@; CS124 add with @ 8. SWG1 change to @ 9. QS4 change to @; RS148,RS149 change to TYPEC@ 10.QC1 change to TYPEC@; RC616,RC617 change to NTYPEC@ 11.RS112,QS6 change to @ 12.Q2509,RC6158,RC6159 change to pop; R2622,R2623 change to @		1.B
8		12/22		1. RO19 remove from BOM. 2. DAZ28Z00102 add into NOTE LIST		1.B
9		12/22		1. PCB Location change to ZZZ1/ZZZ2/ZZZ3 2. D2016,D2017,D2018 change to EMC@		1.B

Security Classification

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2017/12/25

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2019/12/25

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Date

Monday, December 25, 2017

Sheet

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Compal Electronics, Inc.

Title

HW PIR

Rev

1.B

Item	Page#	Date	Request Owner	Issue Description	Solution Description	Rev.
10		12/25		1. PCB change location to ZZZ, and config to PCB1A@,PCB1B@ 2. BOM Loader without HUB@ 3. APU PN update to R3 PN 4. Update Schematic to 1B		1.B

For ACER use